STUDY OF INFRARED SOLID STATE IMAGERS USING CHARGE TRANSPORT DEVICES

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THESIS

STUDY OF INFRARED SOLID STATE IMAGERS
USING CHARGE TRANSPORT DEVICES

by

Ralph Frederick Renzelman, Jr.

December 1974

Thesis Advisor: T. F. Tao

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Study of Infrared Solid State Imagers

Using Charge Transport Devices

by

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Charge Transport Devices (CTD's) for visible imaging have been well developed because of the excellent silicon technology. But infrared CTD imager development has lagged behind because of inherent problems due to an extremely high background photon flux, nonuniformity of detector sensitivities and yet undeveloped infrared metal-insulator-semiconductor (MIS) technology. The purpose of this thesis is two fold. The first was to develop a fabrication procedure for a MIS device for infrared imaging. The TiO_2 insulator would provide large storage capacity for the IV-VI semiconductor, PbTe. Although a complete device wasn't fabricated, significant progress was made in identifying the desirable characteristics and in relative merits of several different approaches. The second part involves a system study comparing the infrared vidicon with CTD's to determine the feasibility of solid state imaging. By comparing these systems it was found that solid state imaging is feasible with improvement schemes such as background suppression and using read only memory or automatic gain control to overcome nonuniformities.

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I. INTRODUCTION

A. INFRARED IMAGING

Infrared imaging is a very important field whose applications have grown greatly in recent years. Applications have spread to military, industrial, medical, and scientific fields. Infrared imaging usually utilizes wavelengths between 1.5 and 14 microns and requires different infrared detector materials to cover different parts of this wavelength spectrum. This range is usually divided into three spectral regions due to carbon dioxide and water molecules absorbing the radiation. These regions or windows are 2.0-2.5μm, 3.5-5.5μm, and 8-14μm. The response of the material depends on the energy gap which is directly related to the wavelength of interest by the relationship:

$$E_g = 1.24/\lambda \quad \text{where } \lambda \text{ is the wavelength in microns}$$

Typical materials are PbS, HgCdTe, and InAs in the 2.0-2.5μm region, InSb, PbTe, PbSe, and HgCdTe in the 3.5-5.5μm region and HgCdTe and PbSnTe in the 8-14μm region.

The major difference between infrared and visible imaging is the level of background radiation present for infrared imaging. Since all parts of a typical natural terrestial scene are normally close to 300°K and since emissivities do not vary greatly, the system must sense extremely small irradiance differences against the prevailing 300°K background. The figure of merit of infrared imagers is therefore based on their contrasts against a large average flux rather than

on their sensitivity to small total photon fluxes against a zero background as is appropriate for camera tubes.

Infrared imaging devices which would utilize charge transport devices (CTD's) instead of bulky, high power consuming vidicons would be highly desirable offering advantages of small size, low weight, low voltage and power requirements. Long range research envisions development of CTO's and detectors of the same material and integrating the two into compact solid state self scanning devices.

B. DEVELOPMENT OF INFRARED IMAGERS

1. Single Element Scanners

Once a detector is developed in a laboratory that will detect over the necessary spectral region, the simplest operational system is the single detector. This system is developed to have a relatively small field of view as the total field of view has to be scanned in a raster type scan. The limit to the field of view is the speed of movement of the target. A further disadvantage of the single element scanner is that there is no integration of the signal flux.

2. Linear Arrays

Once a single element scanner has been developed the next logical step is to design a linear array of elements. Before the CTD was developed these arrays were read out by two methods. The first is to read out the array with an electron beam which means that the system has only one primary amplifier. The second method is to have a separate readout and amplifier for each element of the array.

The early systems of this type were installed in aircraft whose forward flight provided the other dimension to the image. Automatically set into the system was the V/H (velocity/height) ratio which controlled the readout rate of the array. As technology advanced these systems were scanned mechanically in one dimension so they could be used as ground surveillance systems. In these early models the signal was read out onto photographic film so there was no instantaneous readout. An example of an aircraft mounted array is the VKA-702 developed by the Texas Instruments Corporation for the Swedish Air Force. It used cryogenic cooled HgCdTe detectors for imaging in the 8-14μm region.

3. Vidicon

The vidicon is an array of photoconductive targets that are scanned with an electron beam in a small television type camera tube. One end of the evacuated tube is a flat optically transparent faceplate with an inner coating of photoconductive material on top of a transparent electrically conducting signal electrode. In the other end of the tube is the electron gun whose beam is scanned over the photoconductive film by external deflecting coils. The signal electrode is kept at a potential of 20 volts higher than the cathode, and with no signal present, the back of the photoconductive film is kept at the cathode potential by the scanning electron beam. When photons strike the photoconductive film they liberate carriers which changes the film's conductivity, which in turn reduces the potential between

the front and back of the film. When the electron beam reaches the point on the target where photons have struck, electrons are deposited to bring the charge back to its equilibrium condition. The pulse generated by the recharging electrons becomes the signal which is proportional to the number of photons incident on the photoconductive film.

An important advantage of the vidicon is that it is an integrating device. Photons striking the target between electron beam scans change the film conductivity in a small area and therefore are confined to a small area called a resolution element. A sharply focused electron beam reads out one resolution element at a time and therefore each element integrates incident photons for a complete scan period. This period is usually set equal to 1/30 sec to be compatible in standard television.

4. Forward Looking Infrared (FLIR)

Development of FLIR started in 1965 when the military expressed a need to get an instantaneous view of the scene ahead of the aircraft as opposed to an image that had to be photographically developed. Present day FLIR systems give a raster type of the scene similar to that of television. Being an infrared device it is equally useful in night and day, with its limitations being attenuation of infrared in the atmosphere.

In a typical airborne FLIR, the sensor looks at the terrain ahead of the aircraft. The FLIR contains linear arrays of as many as hundreds of infrared detectors which

sense temperature differences within the spectral band, as they are scanned by rotating or scanning mirrors through a field of view. The elevation field of view is covered by the detector array while the scanning action covers the horizontal or aximuth field of view. For each line through which an individual detector is scanned a line can be generated on a cathode ray tube display, providing the operator with a two-dimensional visual presentation of the region viewed by the FLIR sensor.

Outputs from each detector is fed to a high gain amplifier for driving scan conversion equipment to put the final picture into formats suitable for standard or specialized television displays. Scan conversion is doen by electronic multiplexing. Most of the FLIR systems in development today are compatible to modern television's 525 line scan at a frame rate of 30.

Uses of FLIR include sensors in aircrafts, remotely piloted vehicles, missiles, ships (as sensors and navigation aids), and air defense systems.

5. Infrared Solid State Imaging

The present FLIR technology is expected to advance in the future, but a limiting and undesirable feature is the weight and bulk of the mechanical scanning and signal processing equipment. Therefore industry is anxious to exploit features of the CTD's such as self scanning and analog delay elements for use in serial or parallel signal processing. There are two basic approaches to solid state imaging, these being monolithic and hybrid devices.

a. Monolithic Infrared Imaging

The monolithic IRCTD generally uses the standard CTD structure with the substrate consisting of a narrow band gap or an extrinsic semiconductor sensitive to infrared radiation. These devices are further divided up into two more categories.

(1) Inversion Mode Devices. The operation of these devices is similar to the silicon CTD which is based in the generation of an inversion region at the insulator-semiconductor interface where photogenerated minority carriers are collected. The narrow band gap semiconductors are found among binary and tertiary compounds.

(2) Accumulation Mode Devices. A metal-insulator-semiconductor (MIS) structure resulting from application of gate voltage of proper polarity inducing majority carriers at the insulator-semiconductor interface as in the bulk of the semiconductor. Because of this, an extrinsic semiconductor substrate such as gold-doped germanium (Ge:Au) and phosphorous doped silicon (Si:P) can be utilized. The advantage of this is using the well developed silicon technology for both the detector and CTD signal processor.

b. Hybrid Infrared Imaging

Hybrid devices consist of the coupling of any one of the various types of infrared photodetectors to a silicon CCD shift register unit. The signal processing and detection are performed in two distinct units. The signal processing consists of multiplexing, amplification,

correlation, delay, and adding. These devices can be divided into two categories which are described in detail in the next section.

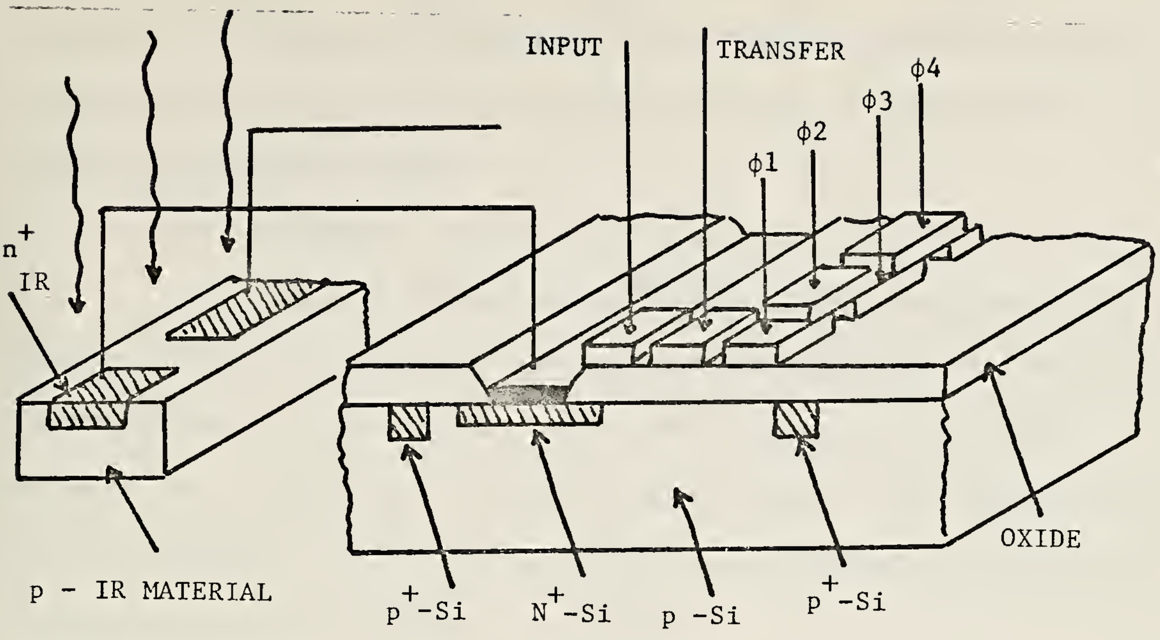
C. PROGRESS OF DEVICE DEVELOPMENT

1. Hybrid Device Development

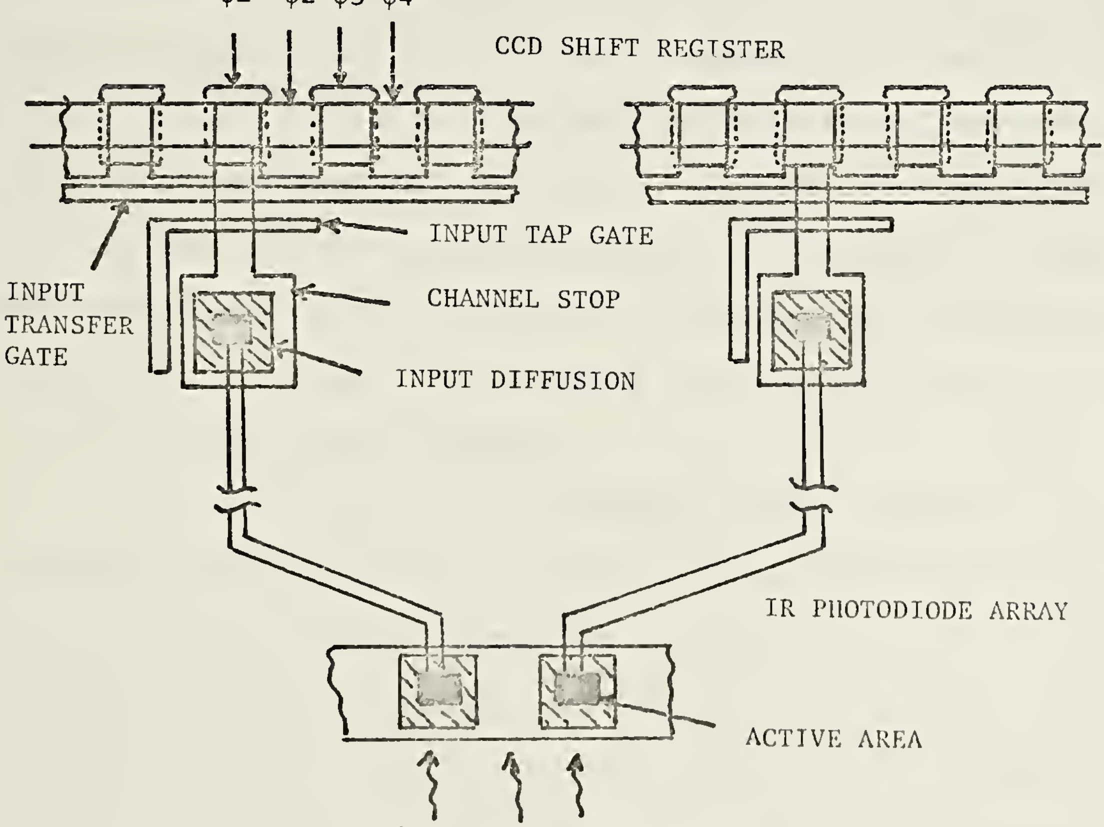
The two different hybrid approaches mentioned previously are now described in detail.

a. Direct Injection Devices

In these devices the photogenerated charge is introduced directly into the CCD shift register. This is shown in figure 1-1 for a n-on-p infrared photodiode and n-channel CCD. The infrared photodiode is connected in parallel to a silicon coupling diode (SCD) diffused into the same silicon substrate on which the CCD is fabricated. The first MOS gate (input) of the CCD is used to reverse bias the infrared diode and the silicon coupling diode; the transfer gate is used to introduce the photocharge into the CCD through a field induced n-channel. When the $\phi 1$ gate is activated with a positive pulse, the potential well under the gate acts as a sink for the diodes and the photocurrent plus the saturation current of the diode will flow into the well for the duration of the $\phi 1$ pulse. When the $\phi 2$ gate is turned on and the $\phi 1$ gate is turned off, the current flow and the charge present is transferred through the device. Rockwell International has developed a direct injection InSb diode array coupled to a 100 bit, p-channel CCD shift



(a) Coupling Concept



(b) Array Layout

FIGURE 1-1 DIRECT INJECTION HYBRID IRCCD

register through eight input taps. The device is operated at 80°K and has been operated at CCD chip frequencies up to and higher than 1 MHZ.

b. Indirect Injection Devices

These devices use a buffer stage between the photodetection stage and the CCD shift register. The composition of the shift registers range from one on-chip MOSFET to a number of off-chip amplifiers. Two applications of the indirect injection devices are with pyroelectric detectors and photoconductive films.

2. Monolithic Device Development

Santa Barbara Research Center, a subsidiary of Hughes Aircraft Company, has reported work on an InSb CCD to demonstrate CCD feasibility by actual measurement of charge transfer. This objective was not met but data from InSb CCDs fabricated and tested indicate that feasibility is in the near future. The problems are not of a fundamental nature but rather are in the fabrication process. It is expected that InSb CCD's will be developed with further process control and fabrication experience.

General Electric has worked almost exclusively with the Charge Injection Device (CID) which works on the same principle as the CCD. They have developed a silicon monolithic camera that they are selling now with 100×100 and 256×188 element arrays. They are attempting to develop a similar type camera in the 1.5-5.5μm region using InSb.

They are attempting to develop a 100×1 array to operate as a 500×500 element array by reading it out in one of the following schemes.

a. Method 1

A linear array is scanned mechanically over the scene to provide a two dimensional image. If, for example, it is desired to have a 500 element linear array, it is made up of five 100 element arrays each of which is read out into its own amplifier. Therefore, the system requires five preamplifiers.

b. Method 2

A two dimensional area array (m×n) is made up of m linear arrays of n elements each. This scheme eliminates problems associated with mechanical scanning. Since the background flux is high various schemes have to be used to overcome saturation of the elements during the frame time.

(1) The m linear arrays can be sequently read in parallel. Because of this the frame rate is m times faster than the frame rate for an area array.

(2) The line arrays can be sequently enabled and read, thereby achieving an integration time which can prevent saturation and yet maintain the original frame rate.

D. NONUNIFORMITY AND SYSTEM STUDY

It has developed that the limiting factor in most imaging applications is the nonuniform sensitivities between adjacent detector elements. This problem of nonuniformity has slowed down advancement of infrared arrays over the past

few years. In the third part of this thesis a system study will be presented to discuss different methods of overcoming this problem of nonuniformity.

E. THE IV-VI AND HIGH DIELECTRIC CONSTANT SI-MIS

In fabricating a IV-VI MIS for infrared imaging in the 8-14μm region it is desirable to develop a high storage capacity because of the high background present in this region. Therefore a high dielectric constant insulator is needed. This is because

$$Q_s = V_g(C_{ox}-C_{DD}) \tag{1}$$

where

V_g = gate voltage

C_{ox} = capacitance of the insulator

C_{DD} = capacitance in deep depletion

The variable that can be changed with greatest effect is the oxide capacitance which is equal to:

$$C_{ox} = k\varepsilon_0 A/d \tag{2}$$

where

k = dielectric constant

ε_0 = permittivity of free space

A = area of the gate

d = thickness of the insulator

To increase this, d can be made smaller but is limited by the breakdown voltage. The area of the detector is usually controlled by the size of the array and spatial resolution

required. Therefore the only thing left to alter is the dielectric constant of the insulator. In this research it was decided to develop titanium dioxide and tantalum pentoxide for insulators. To set up developing procedures and to establish standards, it was decided to start depositing TiO_2 on silicon. This was because we understand very well the surface properties of silicon in these TiO_2-Si devices. Therefore, we can concentrate our attentions to the properties of the insulator. This will have another practical pay off in developing a large storage capacity for silicon.

II. MIS DEVICE DEVELOPMENT

A. BACKGROUND

A survey of past work on MIS devices can be broken up into two categories, silicon-MIS and other MIS devices.

1. Silicon MIS

Extensive work has been done with the natural oxide of silicon, SiO_2. Other insulators have been used to increase the storage capacity. These insulators include Al_2O_3, TiO_2, and Si_3N_4.

2. MIS of Other Semiconductors

In the 3-5μm region using III-V semiconductors Santa Barbara Research Center and General Electric have worked with InSb. GaAs and GaAsP as well as many silicon devices have been investigated by the University of New Mexico. In the IV-VI region MIS devices have been investigated at the Naval Postgraduate School under the supervision of Dr. T. F. Tao.

B. THEORY OF MIS

This is a theoretical study of a single MIS device to determine its feasibility for use as an infrared CCD. The basic cell of the CCD is the MIS. This means that the basic element of a CCD is 2, 3, or 4 MIS cells depending on whether the CCD is phased in 2, 3, or 4 phases.

1. The Ideal MIS Structure

The ideal MIS analysis considered will contain no interface states (N_{ss}), no metal-to-semiconductor work function differences (ϕ_{ms}), and negligible bulk semiconductor resistance and insulator conductance. Under zero bias conditions the energy band structure is shown in Figure 2-1. Here the metal-to-semiconductor work function (ϕ_{ms}) is equal to zero and is represented by

$$\phi_{ms} = \phi_m - (\chi + E_g/2q - \psi_B) = 0 \text{ for n-type} \qquad (3)$$

$$\phi_{ms} = \phi_m - (\chi + E_g/2q + \psi_B) = 0 \text{ for p-type} \qquad (4)$$

where

ϕ_m = metal work function

χ = semiconductor electron affinity

ψ_B = potential difference between Fermi level E_F and intrinsic Fermi level E_i

E_g = energy band gap

E_c = energy in the lower edge of the conduction band

E_v = energy in the upper edge of the valence band

q = charge in an electron

After a device is biased with positive or negative voltage three different cases occur in the MIS: accumulation, depletion, and inversion. The energy band diagrams for these three cases are shown in Figure 2-2 for n and p types.

In a p-type MIS with negative bias applied with respect to the substrate, the top of the valence band bends

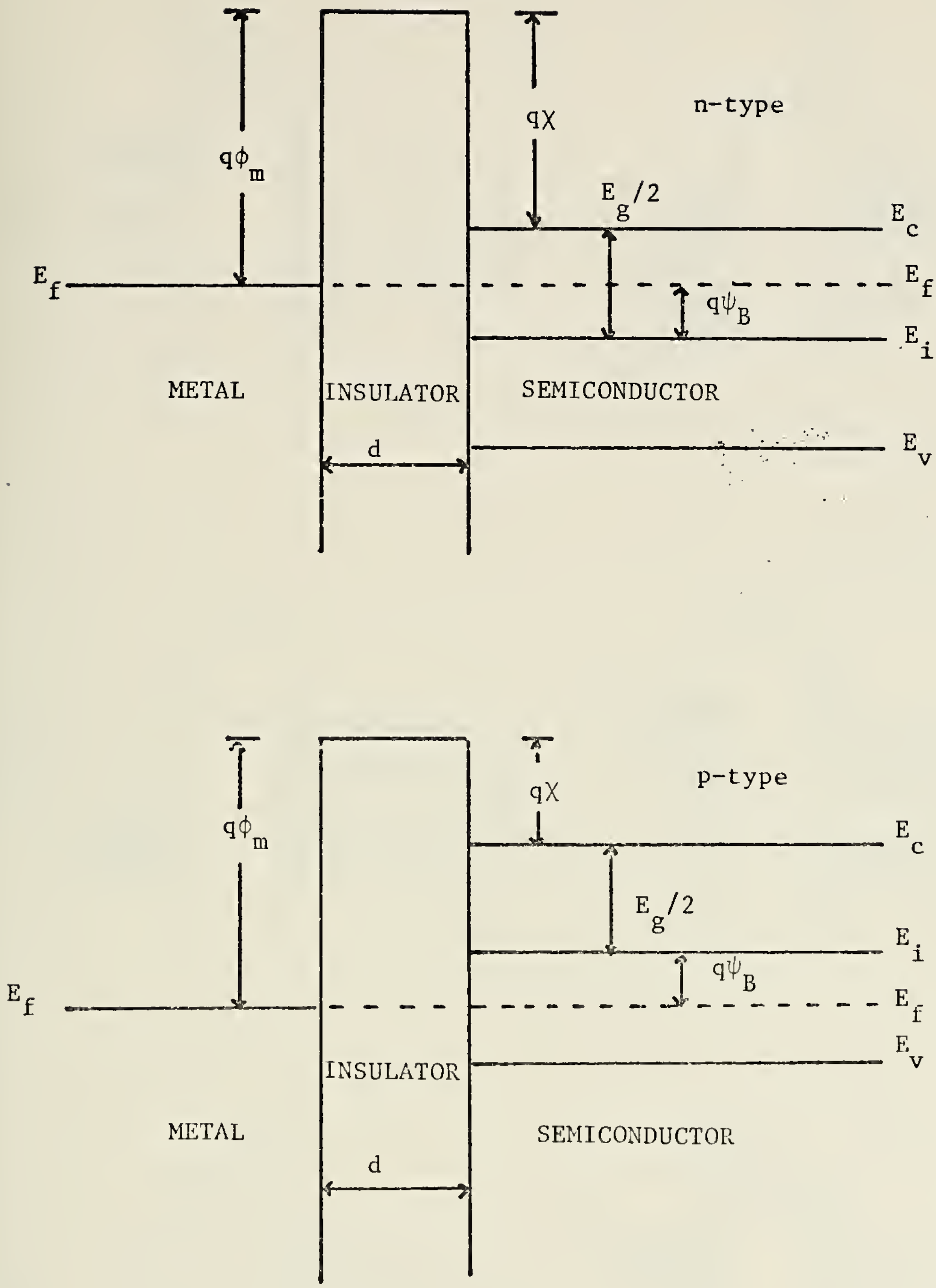


FIGURE 2-1

AN IDEAL MIS BAND DIAGRAM AT ZERO BIAS

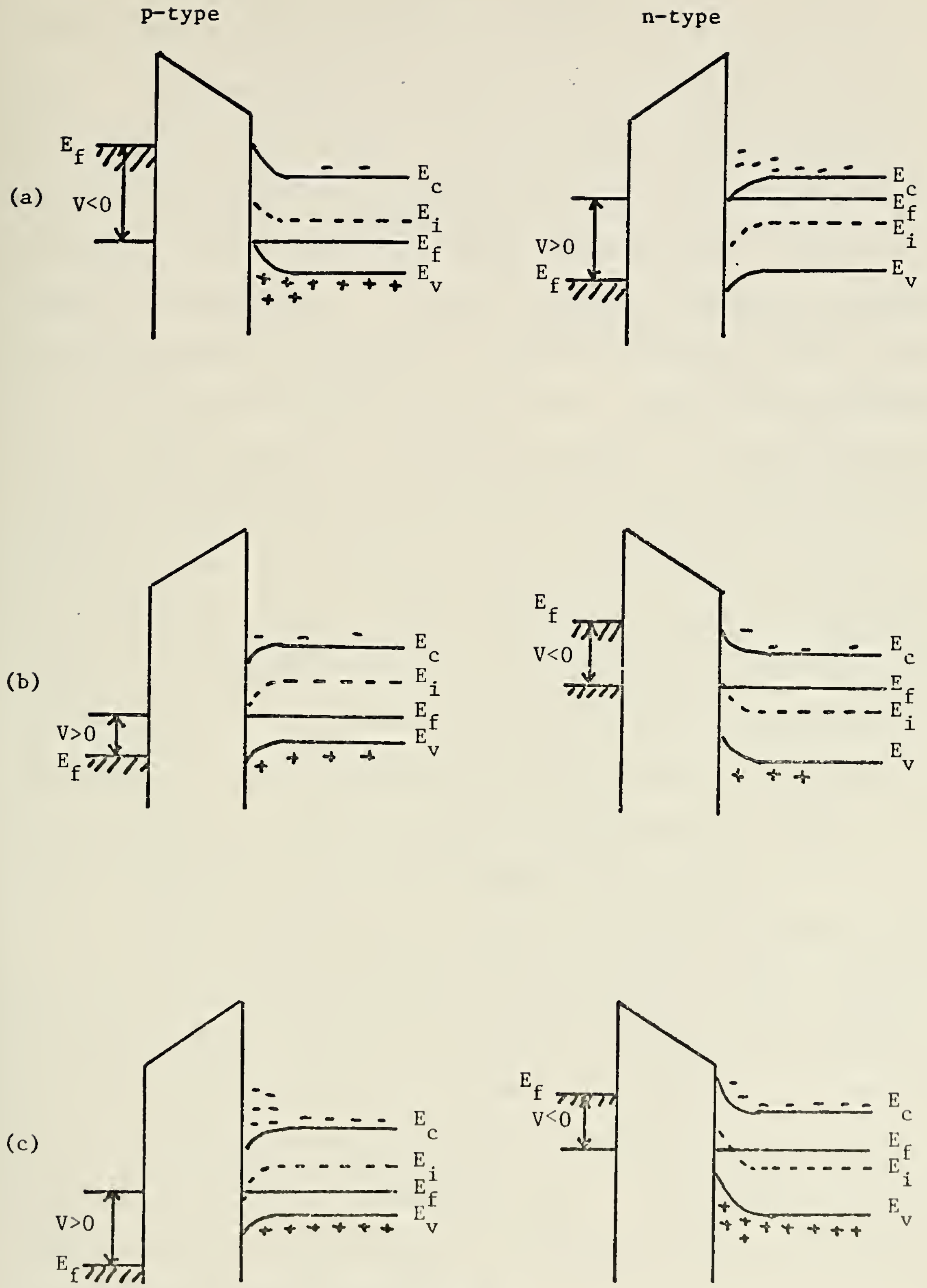


FIGURE 2-2

BAND DIAGRAMS AT (a) ACCUMULATION, (b) DEPLETION, (c) INVERSION

upward and is closer to the Fermi level. Since there is no current flow in an ideal MIS the Fermi level remains constant. This bending of the band causes the majority carriers, in this case holes, to be attracted to the interface between the semiconductor and insulator by the attractive forces of the net negative charge on the gate. This is called "accumulation". A small positive voltage is applied to the gate and the majority carriers are pushed away from the surface forming a depletion area. This bending downward of the energy bands is called "depletion". As more positive voltage is applied the energy bands are bent down even further until the intrinsic level E_i at the surface crosses over the Fermi level. This attracts the minority carriers (electrons) to the interface thus forming an inversion layer as they now out number the majority carriers. The n-type semiconductor acts the same way except that the majority carriers are electrons and minority carriers are holes. This case is referred to as low frequency inversion.

Two other cases must also be considered; these being high frequency inversion and deep depletion. High frequency inversion occurs when the a-c signal is applied so rapidly that the minority carriers cannot be supplied by the generation and recombination rates in the semiconductor. This results in a partial inversion case. In the deep depletion case the dc bias sweep and a-c signal are both so rapid that no inversion takes place.

2. Charge Distribution in a MIS Structure

The charge per unit area on the metal (Q_m) must equal the total charge per unit area in the semiconductor (Q_s) for all bias voltages. The applied voltage is divided between the insulator and semiconductor. The capacitance of the insulator is constant and given by equation (2). The capacitance of the semiconductor (C_s) is voltage dependent of the charge distribution in the semiconductor.

Figure 2-3 shows the charge distribution as a function of distance x for a MIS in the three states described above; accumulation, depletion, and inversion. Here the space charge is given by

$$Q_s = \int_{x=0}^{\infty} \rho(x)dx \tag{5}$$

where

$\rho(x) = q(p - n + N_D - N_A)$

p,n = carrier concentrations

N_D, N_A = impurity concentrations

The charge in the depletion layer and in the inversion layer as a function of surface potential requires the integration of a one-dimensional Poisson equation and with substitution of Gauss' Law yields

$$Q_s = -2\frac{U_s}{|U_s|} q n_i L_D \{2[\cosh(u_s - U_b) - \cosh(U_b) + U_s \sinh(U_b)]\}^{\frac{1}{2}} \tag{6}$$

where

U_s, U_b are the potentials at the surface or bulk of the semiconductor. This is in kT/q units.

$$L_D = (kT\varepsilon_s/2q^2 n_i)^{\frac{1}{2}} = \text{the intrinsic Debye length} \tag{7}$$

The inversion layer contribution to Q_s is Q_n given by a second integration of Poisson's equation yielding

$$Q_n = -\left|\frac{U_s}{U_s}\right| q n_i L_D \int_{U_b}^{U_s} \frac{\mathrm{EXP}(U-U_b)du}{2[\cosh(U-U_b)-\cosh(U_b)+\sinh(U_b)]^{\frac{1}{2}}} \tag{8}$$

Q_s can now be written in terms of Q_n and x_d, the effective depletion width.

$$Q_s = Q_n + q(N_D-N_A)x_d \tag{9}$$

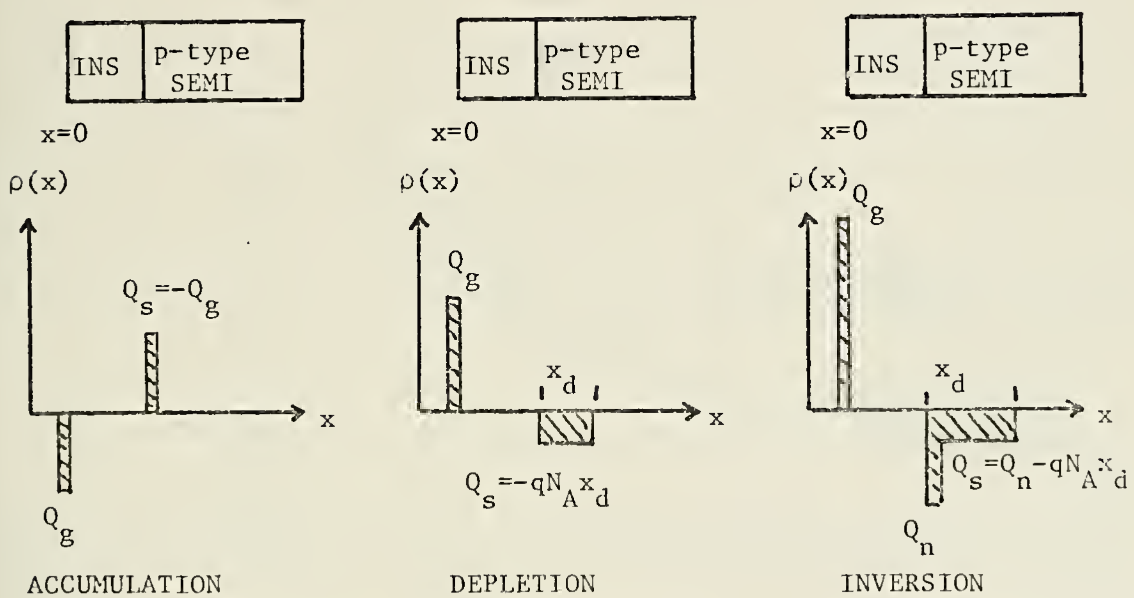


FIGURE 2-3 PLOT OF CHARGE VERSUS DISTANCE IN A MIS

3. <u>Capacitance-Voltage Characteristics of an Ideal MIS</u>

A typical capacitance versus gate voltage curve is shown in figure 2-4 for a p-type semiconductor. The capacitance is proportional to the voltage (Q=CV) and charge.

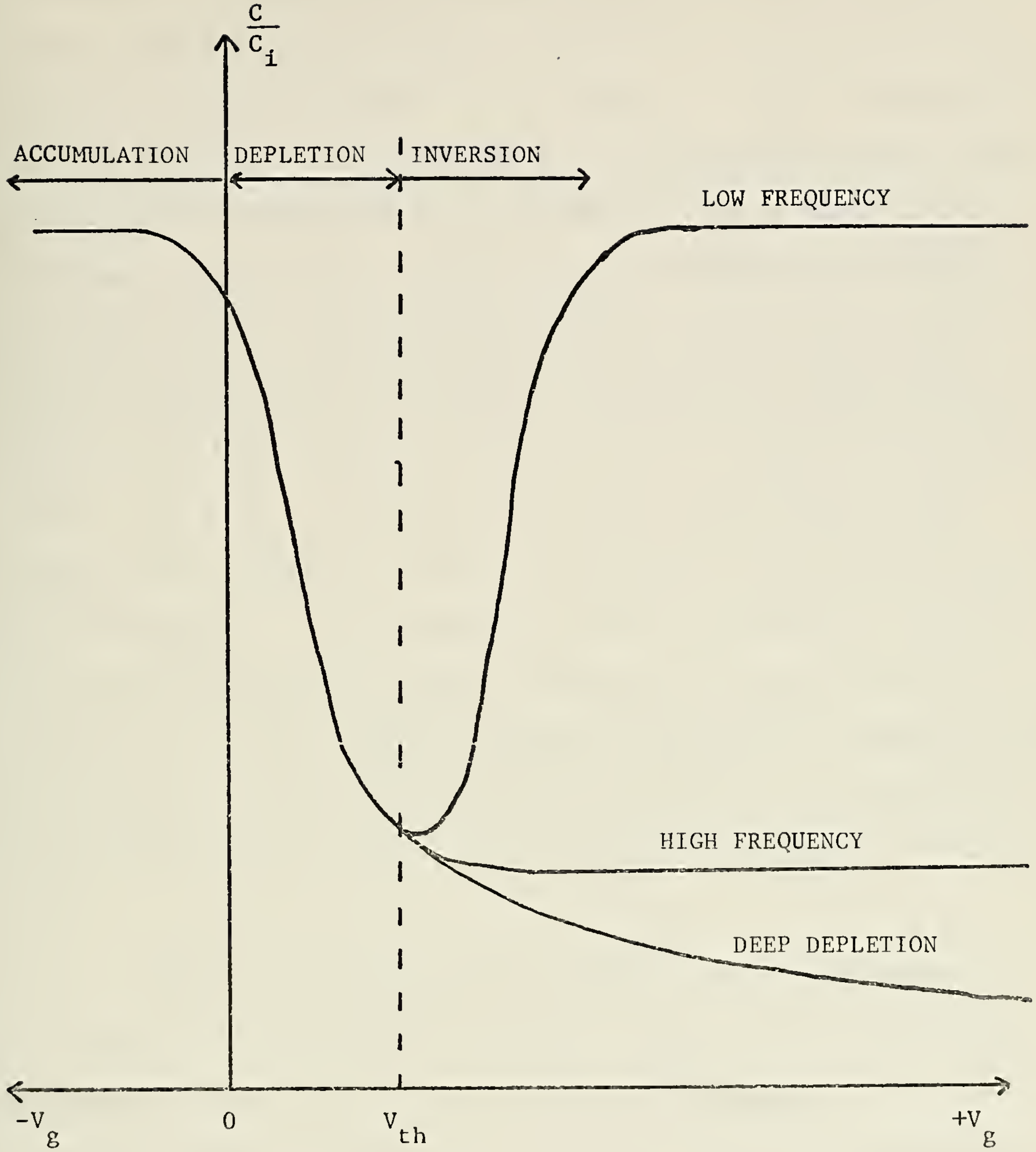


FIGURE 2-4 IDEAL C-V CURVES FOR P-TYPE MIS

Therefore, the different regions can be described by referring to the previous section. Notice that the capacitance is normalized to the oxide capacitance. In the accumulation region, there is an accumulation of holes in the semiconductor insulator interface and therefore a large capacitance. Applying a more positive bias leads to reduced hole density and formation of the depletion layer. Since this region contains practically no carriers and acts as a dielectric in series with the insulator resulting in a lower total capacitance. The C-V curve passes through a minimum and then rises to the inversion layer as minority carriers form at the interface. If the change in signal frequency is high the minority carriers cannot form and the capacitance remains low. If the signal voltage is applied so rapidly that no minority carriers form at the interface the capacitance further decreases in value and in theory eventually goes to zero.

Using the equations for charge in the semiconductor developed in the previous section, the following equations for capacitance in each region can be developed. Since the MIS model is two capacitors in series, the total capacitance is

$$C_t = \frac{C_i C_s}{C_i + C_s} \quad \text{or normalizing} \quad \frac{C_t}{C_i} = \frac{1}{\frac{C_i}{C_s} + 1} \tag{10}$$

For the low frequency case,

$$C_s = \varepsilon_s \frac{q(p-n+N_P+N_A)}{Q_s} \tag{11}$$

where the minority carriers can follow the applied bias and signal.

In the high frequency inversion case, an effective depth X_{eff} must be considered since the minority carriers don't follow the ac signal but are none the less affected by it. Therefore,

$$C_s = \frac{K_s \varepsilon_s}{X_{eff}} \tag{12}$$

where

$$X_{eff} = \int_0^{U_s} \frac{1-e^u}{[\cosh(U_s-U_b)-\cosh(U_b)+U_s \sinh(U_b)]} du$$

This value of C_s is then substituted into equation (10) for the total capacitance.

In the high frequency deep depletion case, the C-V relationship is like that of a reverse biased pn junction. This is really a transition case in which the MIS is not in equilibrium and can be caused by a leaky oxide or if the dc bias is rapidly swept from accumulation to inversion. The capacitance is again given by equation (10) where X_{eff} is a different value since there is no inversion layer and $Q_s = q(N_D - N_A)X_{eff}$. The deep depletion capacitance is

$$\left.\frac{C}{C_i}\right|_{DD} = \frac{1}{1+[2K_i^2 \varepsilon_0 V_g / q(N_A - N_D) K_s X_i^2]} \tag{13}$$

4. Capacitance-Time Characteristics of an Ideal MIS

When a MIS device is pulsed into deep depletion from accumulation the semiconductor surface potential is large at the onset of depletion and then relaxes to some quasi-equilibrium inversion value in a certain characteristic time, T. The length of this time T depends on the rate at which the majority carriers drift to the bulk region to neutralize the ionized acceptor atoms and on the rate of minority carrier generation at the interface. A number of parameters can be derived from a plot of C versus t, among these diffusion length, minority carrier lifetime, surface generation velocity, storage time and a measure of the maximum amount of charge that can be stored.

Figure 2-5 shows the relationship between a pulsed waveform, C-V characteristics, and C-t characteristics.

The two more important parameters of a MIS derived from a C-t curve are storage time and storage capacity. The storage time is defined as the maximum amount of time that a MIS will remain in deep depletion once pulsed. This time sets the lower limit on the clock frequency. Incidently, long storage times are favorable in CCD applications since it allows fewer unwanted non-signal carriers to enter into inversion.

Storage capacity is the maximum amount of minority charge that can be stored in each MIS element. One estimate of this storage capacity is

$$Q_{stor} = (C_{inv} - C_{DD})V_{inv} \tag{14}$$

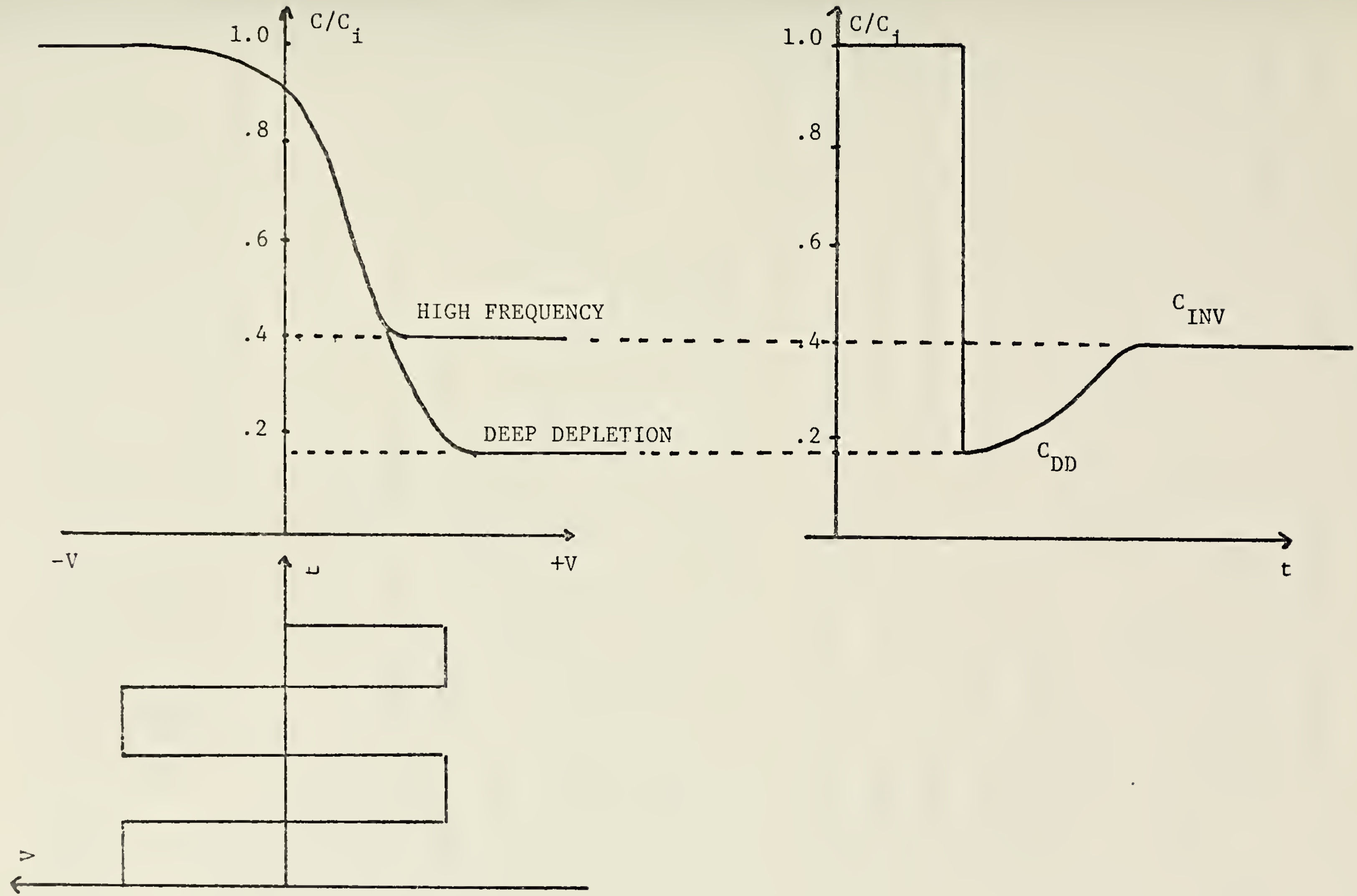


FIGURE 2-5 RESPONSE OF A MIS TO PULSING FROM ACCUMULATION TO DEPLETION

5. <u>The Non-Ideal MIS Structure</u>

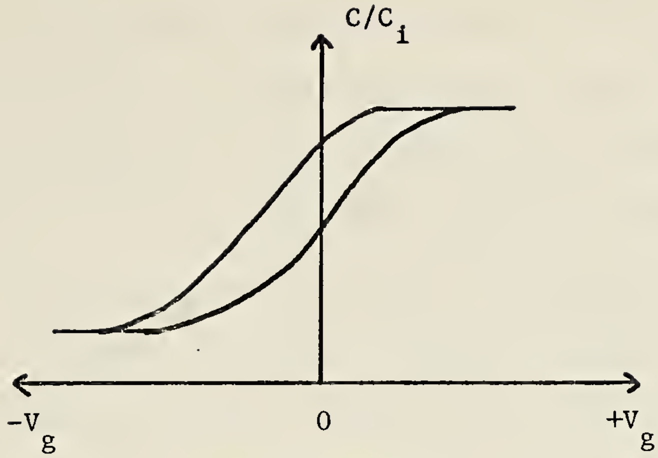
The fabrication of MIS devices and the physical parameters of the materials involved introduce factors that cause deviations from the ideal characteristics. These deviations are important in understanding experimental results of the MIS work and are described below.

a. Metal Work Function

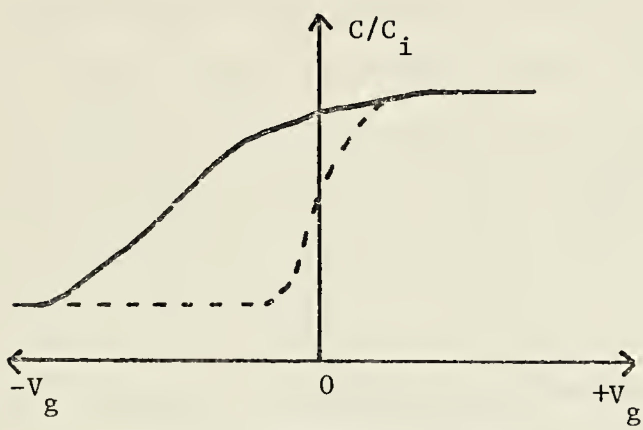
If the value of the work function (ϕ_{ms}) is other than zero (the sign depending upon whether the MIS is p or n type), the experimental C-V curve will be displaced right or left by an amount equal to ϕ_{ms}. This isn't really a serious problem as the displacement can be easily calculated and the curve shifted back.

b. Charges in the Insulator

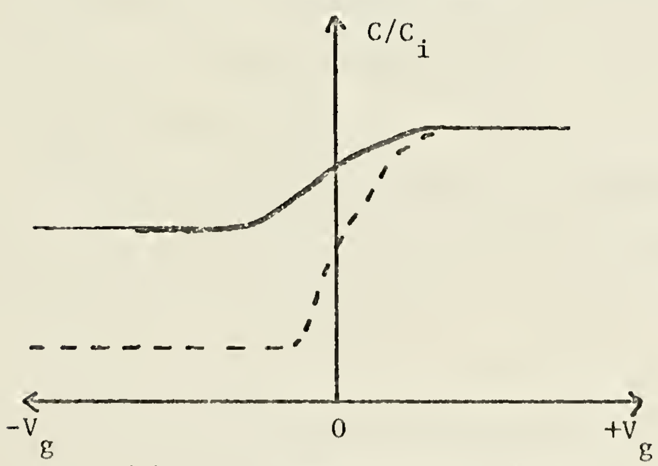
There are two types of charges introduced during fabrication of the insulator, these being fixed and mobile charges. The fixed charges are located at or near the semiconductor surface and are immobile with an applied field, but a portion of the bias field is required to neutralize the effect of the fixed charge. This causes the experimental C-V curve to shift without distortion. However, the mobile ions tend to follow the variation of the applied field but at a slower rate than the carriers. This results in a hysteresis effect which is shown in figure 2-6a. Hysteresis means that a curve generated by a positive to negative voltage differs from that generated by a negative to positive voltage.



(a) HYSTERESIS



(b) INTERFACE STATES



(c) HIGH CONTACT RESISTANCE

FIGURE 2-6 C-V CHARACTERISTICS OF NON-IDEAL MIS

c. Interface States

An interface state is defined as an allowed energy level within the forbidden gap at the surface. There are two possible states, these being donor states and acceptor states. A donor state can have two states of charge; these being neutral or positive due to giving up an electron. This state of charge is controlled by the Fermi level -- being in its positive state when above the Fermi level. The acceptor conversely changes its state from neutral to negative. As external bias is applied to the MIS the bands tend to bend and the surface state levels move with the valence and conduction bands while the Fermi level remains fixed. The change in charge comes about when the interface state crosses the Fermi level, which in turn changes the MIS capacitance. This change of capacitance (ΔC) is shown in figure 2-6b and gives three different effects. This gives additional capacitance, a frequency dispersion, and they change the voltage axis by changing the dependence of the surface potential on the applied bias.

d. Ohmic Contacts

If there is a high contact resistance on the leads to a MIS device the C-V curve is distorted as in figure 2-6c.

C. EXPERIMENTAL PROCEDURES

1. Fabrication

a. Semiconductor

Thin films of PbTe were grown and the techniques learned from this can be readily expanded to grow PbSe, $Pb_xSn_{1-x}Te$, and $Pb_xSn_{1-x}Se$ thinfilms. Different stoiciometric combinations were tried to control carrier concentrations of the thin films and were prepared in the following way.

High grade purity lead and tellurium were carefully measured with the weights dependent on the stoiciometric concentration desired, i.e. $Pb_{1.001}Te$. The lead was poured into a quartz tube that had been cleaned with dichromate acid and rinsed in distilled water. The tube was 2" in diameter and 6" long with two smaller quartz tubes proturding from the ends. The lead was then melted and cooled to solidify it. The pelletized tellurium was then added to the quartz boat. The quartz boat was installed on a vacuum system which was used to draw purified hydrogen gas continually through the boat as the tellerium was melted. The quartz boat was then sealed at both ends under a vacuum leaving the contents under a pressure of 3×10^{-6} torr. The boat was then left in a furnace for 12 hours at a temperature of 1180°C.

The thin films were deposited in a specially constructed furnace. The substrate holder was a 3/4" carbon slug 1" long with a slot drilled in one end just large enough for the substrate to fit into and be flush with the end.

This slug fitted into a barium nitrate heater slug 2" in diameter around which was wound nickel chromium wire. The furnace was a quartz tube 2½" long with the top rolled over into a rim to prevent it from slipping through the heater coils. The complete furnace consisted of the substrate heater/holder suspended 2" above the furnace with a chimney in between to prevent contamination of the vacuum chamber and a flapper to "turn" the furnace on and off.

Barium flouride was used as the substrate for all thin films grown. It was found that the substrate temperature had to be very carefully controlled during deposition or cloudy films resulted. The temperature range found best was 320-330°C. The source furnace temperature was not monitored accurately and deposition rate was controlled by the current through the heater coils. A furnace temperature of approximately 600°C yielded a growth rate of approximately two microns per hour. A Hall mask was used to grow the films in the shape of figure 2-7.

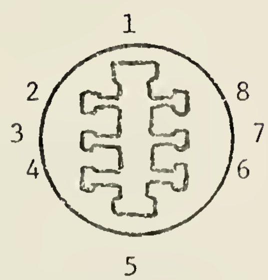


FIGURE 2-7 HALL MASK USED IN DEPOSITION

Metallurigical measurements were made on the samples in order to determine their crystal structure and orientation. Specific tests were Louie photographs and electron diffraction. Thickness of the films was determined by a Perkins Elmer spectrometer. Leads were then epoxied onto the Hall sample with silver epoxy and Hall measurements were performed. Basically, these consisted of a liquid nitrogen cold finger onto which the sample is mounted and then placed between two magnetic poles. The polarity and change of voltage measured between contacts 3-7 in figure 2-7 determined the Hall voltage and whether the semiconductor was p or n type. The conductivity voltage was also monitored as the sample was cooled from room temperature to 77°K. Using these voltages the following values can be obtained using these formulas:

$$R_H = 2V_H t$$

$$n/p = 1/R_H q$$

$$\sigma = \frac{1}{\rho} = \frac{i}{tV_\sigma}\left(\frac{\ell}{w}\right)$$

$$\mu = R_H \sigma$$

definition of terms;

R_H = the Hall coefficient

V_H = Hall voltage

t = semiconductor thickness

q = charge of an electron

n/p = the majority carrier of the semiconductor

σ = conductivity of the semiconductor

μ = mobility of the semiconductor

ℓ = length between measuring points (2-4)

w = width of the Hall sample between points (3-7)

b. Insulator

It was attempted to fabricate an insulator layer of TiO_x. This consisted of depositing titanium on a glass slide with a Varian 2kw e-gun and monitoring the deposition rate with a Sloan Rate Monitor. This was carried out successfully with films grown ranging from 1000-15000Å. The next step was the anodization phase. Oxalix acid was used as the bath, a platinum wire acted as the cahtode, and the titanium thinfilm served as the anode. A constant current power supply was used which had a maximum voltage capability of 150-200 volts. Figure 2-8 shows a block diagram of the anodization procedure.

c. Metal Contacts

Gold or aluminum were deposited on the samples in a separate vacuum system consisting simply of a high current feed through and a small wire basked wound in the shape of a cone and approximately ½" high. Pieces of sputtered gold or aluminum were inserted into the basket and the appropriate mask placed over the devices at which point the system was pumped down to 3×10^{-6} torr. As the power supply connected to the small basket was turned up the basket heated up and melted the gold or aluminum. Since each have good wetting properties the molten metal stayed in the baskets and as more current was applied the metal evaporated

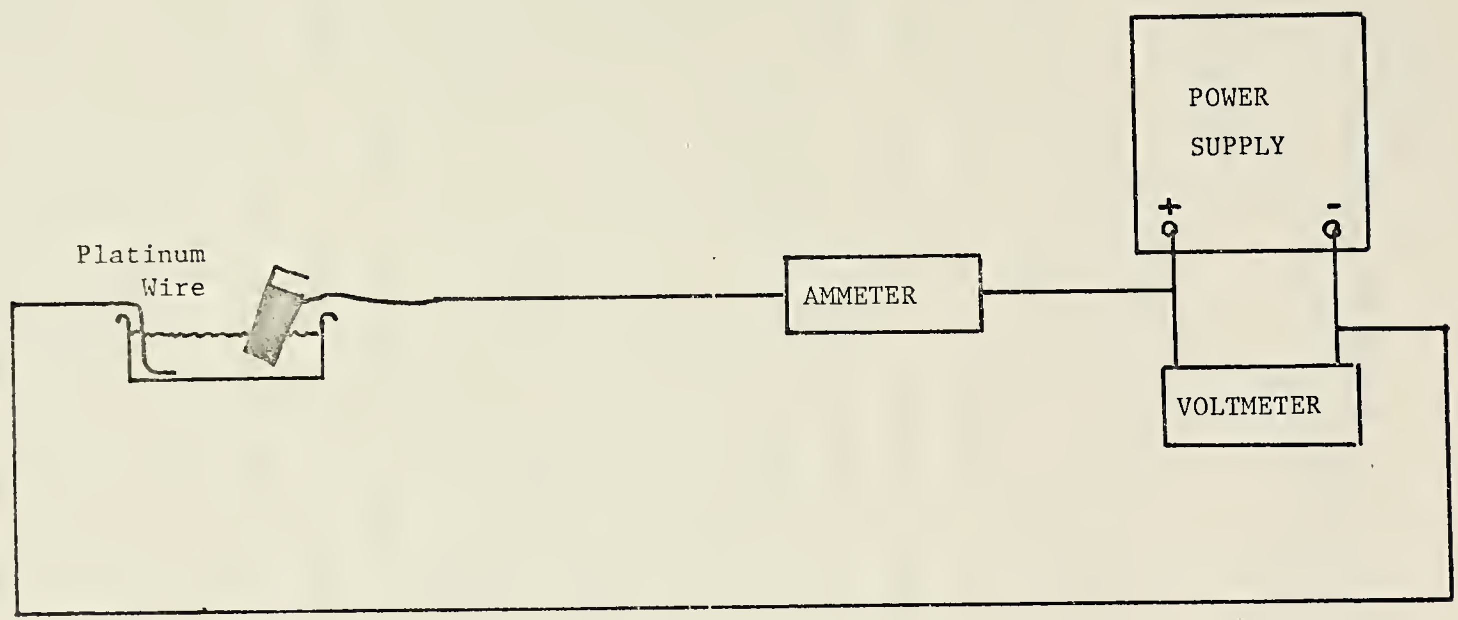


FIGURE 2-8 BLOCK DIAGRAM OF ANODIZATION PROCESS

and was deposited on the device approximately 12" above the basket.

2. Testing

To evaluate the MIS devices fabricated, two basic tests need to be taken. These are measuring the C-V and C-t characteristics.

a. C-V Characteristics

Only high frequency C-V characteristics were measured to get a rough idea of device characteristics. Figure 2-9 shows a block diagram of the experimental set-up used. The Boonton Model 72A Capacitance Meter was used as it provides a direct scale readout on a X-Y recorder output for full scale capacitance ranges of 1,3,10,30,100,300,1000, and 3000 picofarads. The bias voltage was applied which could range from ±200, ±400, or ±600 volts dc. The bias voltage combined with the internal 15mv-1MHZ signal to allow the MIS device to be swept through plus and minus voltages. A Wavetek Model 142 was used to provide a triangular waveform to the sample through the capacitance meter. A dc power supply was used to apply external bias to the Wavetex to shift the triangular waveform above and below zero. An X-Y recorder was used to record the subsequent C-V curves.

A Boonton Model 75 Bridge was used during C-V measurements to spot check capacitance and measure device conductance. An advantage of this device is that the measuring frequency could readily be changed but unfortunately dc bias was limited to less than five volts. The sample was

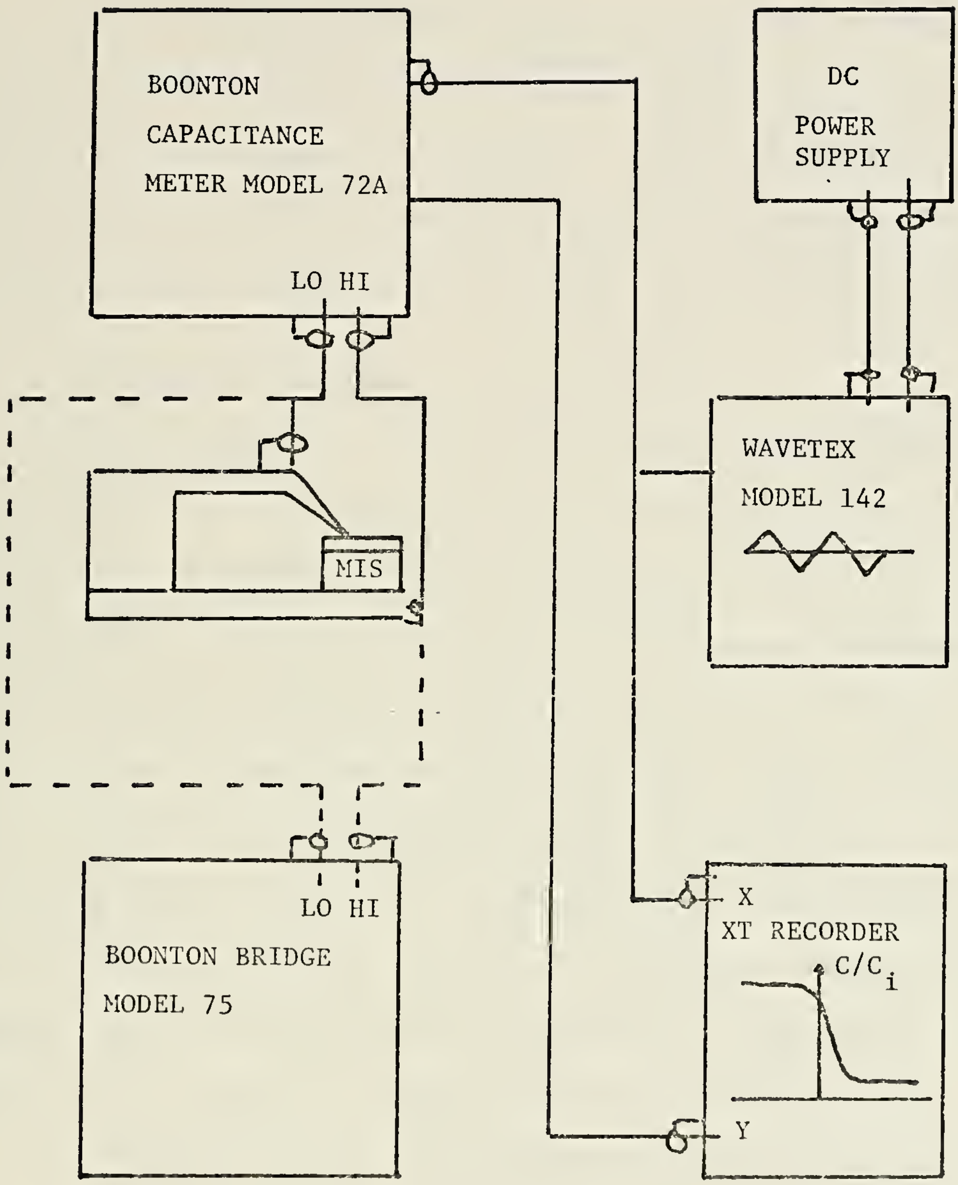


FIGURE 2-9

BLOCK DIAGRAM FOR MEASURING C-V AND C-t CHARACTERISTICS

mounted in a probe so that the metal dots could be probed at random.

b. C-t Measurement

The same block diagram of figure 2-9 was used to measure C-t characteristics except the Wavetex signal generator was in the square wave mode. The resulting C-t curve was traced on the X-Y recorder unless the storage time was so short that it had to be recorded on an oscilloscope.

D. EXPERIMENTAL RESULTS I - SILICON MIS

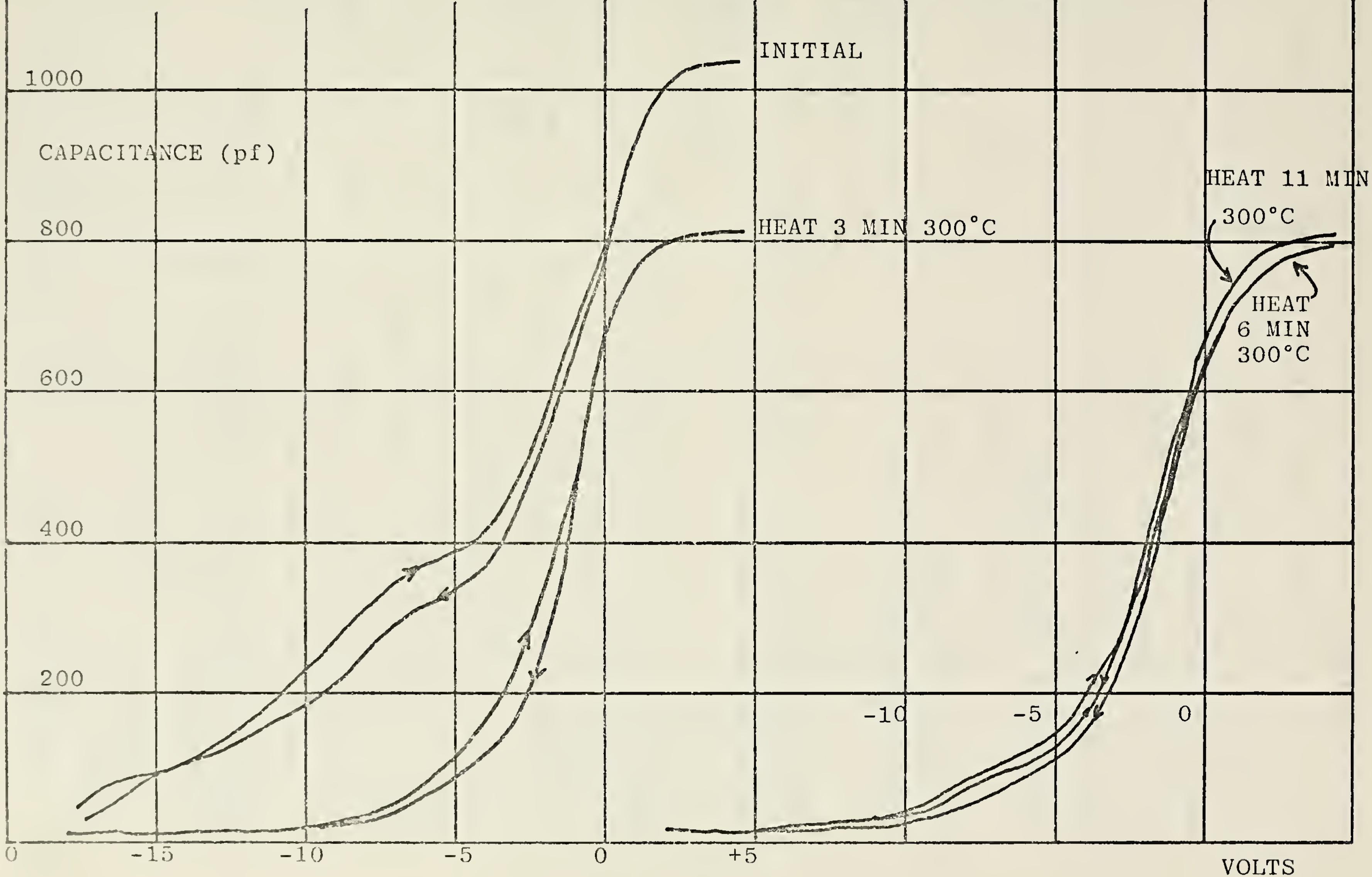
The MIS capacitors were fabricated by a reactive sputtering process in pure oxygen atmosphere back filled to approximately ten microns of partial pressure. These consisted of two batches. The first batch was MIS capacitors having 1500Å of TiO_x deposited on n-type silicon (3-5Ω-cm). The second batch consisted of four different types of MIS capacitors: n-type Si-4100Å TiO_x, p-type Si-4100Å TiO_x, n-type Si-9000Å TiO_x, and p-type Si-9000Å TiO_x. The resistivities are all in the 3-5Ω-cm range. C-V data was taken on these samples and various methods of post heat treatment were then used in an attempt to improve these characteristics.

1. Results of the First Batch of TiO_x-Si Capacitors

Looking at the initial C-V curve the following conclusions can be drawn (see figure 2-10).

(a) By measuring the area of the MIS capacitor and thickness of the insulator a dielectric constant of 25-30 is obtained. This is slightly lower than expected because the

Figure 2-10 First Batch C-V Curves n-type Si - 1500Å TiOx



sputtered oxides of titanium are not the stoichiometric TiO_2. Instead, it should be described more appropriately as TiO_x.

(b) The TiO_x was deposited on a two inch wafer of silicon. From the changes in color of the oxide from blue to a deep violet, it is known that the composition and thickness of the oxide varies over this wafer. These differences in oxide can also be detected by examing the C-V characteristics. Figure 2-11 is an example of this.

(c) There is a small hump in the C-V curve near the inversion threshold indicating trapped charge states near the valence band.

(d) Hysteresis is common in all samples in varying degrees. The amount of hysteresis has been reduced by post heat treatment.

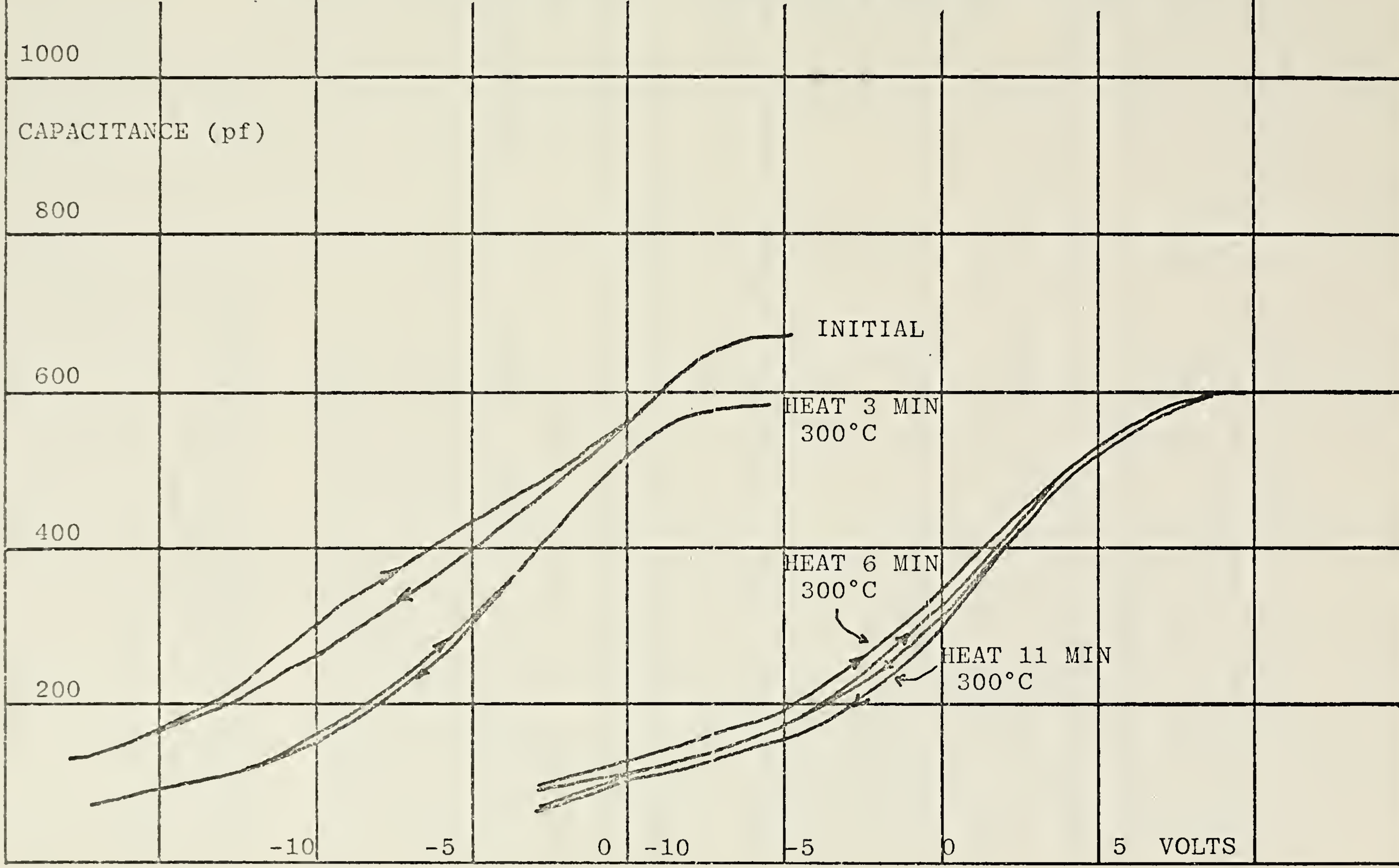
(e) The voltage bias ranges over which the accumulation state is changed to inversion state typically vary from five to ten volts which is much larger than theoretical analysis would indicate, (less than five volts).

(f) The value of capacitance measured on the Boonton Bridge, Model 75, agrees closely with the Boonton Capacitance Meter, Model 72, for these samples. Their typical shunt resistance values are in the range of 3-5000 ohms.

2. <u>Results of the First Batch Following Heat Treatment</u>

By heating the samples in a nitrogen atmosphere at 300°C, the C-V characteristics were generally improved. Figure 2-10 shows the results of one of the better samples after heat treatments of three, six, and eleven minutes. It

Figure 2-11 First Batch C-V Curves n-type Si - 1500Å TiOx



can be seen that after the initial three minutes of heat treatment no further improvement is observed. The sample was then heated in an oxygen atmosphere at 300°C in an attempt to investigate whether the presence of oxygen in heat treatment is an important factor or not. The results are quite similar to those with heating in nitrogen indicating that the heat treatment is not really an oxidation process.

The same heat treatment was tried on samples with poorer initial C-V characteristics (see figure 2-11). The results indicate the same trend of improvements. It is interesting to note that in all cases heating reduced the capacitance of the oxide. Since the MIS area and the insulator thickness remained the same, it would seem that the dielectric constant decreased in value upon heating.

The effects of electric field during heat treatment were investigated by heating the samples while a voltage was being applied. So far this series of measurements has not yielded significantly different results. It is not in agreement with the experiences in the SiO_2 trade where it is generally known that electric field during heating helped in moving the charges in insulators and reducing the hysteresis and drift effects.

3. Results of the Second Batch of TiO_x-Si Capacitors

The second batch of MIS capacitors was not nearly as successful as with the first batch. The initial C-V curves for two samples are shown in figure 2-12. As can be seen they exhibit all the bad characteristics of the first batch

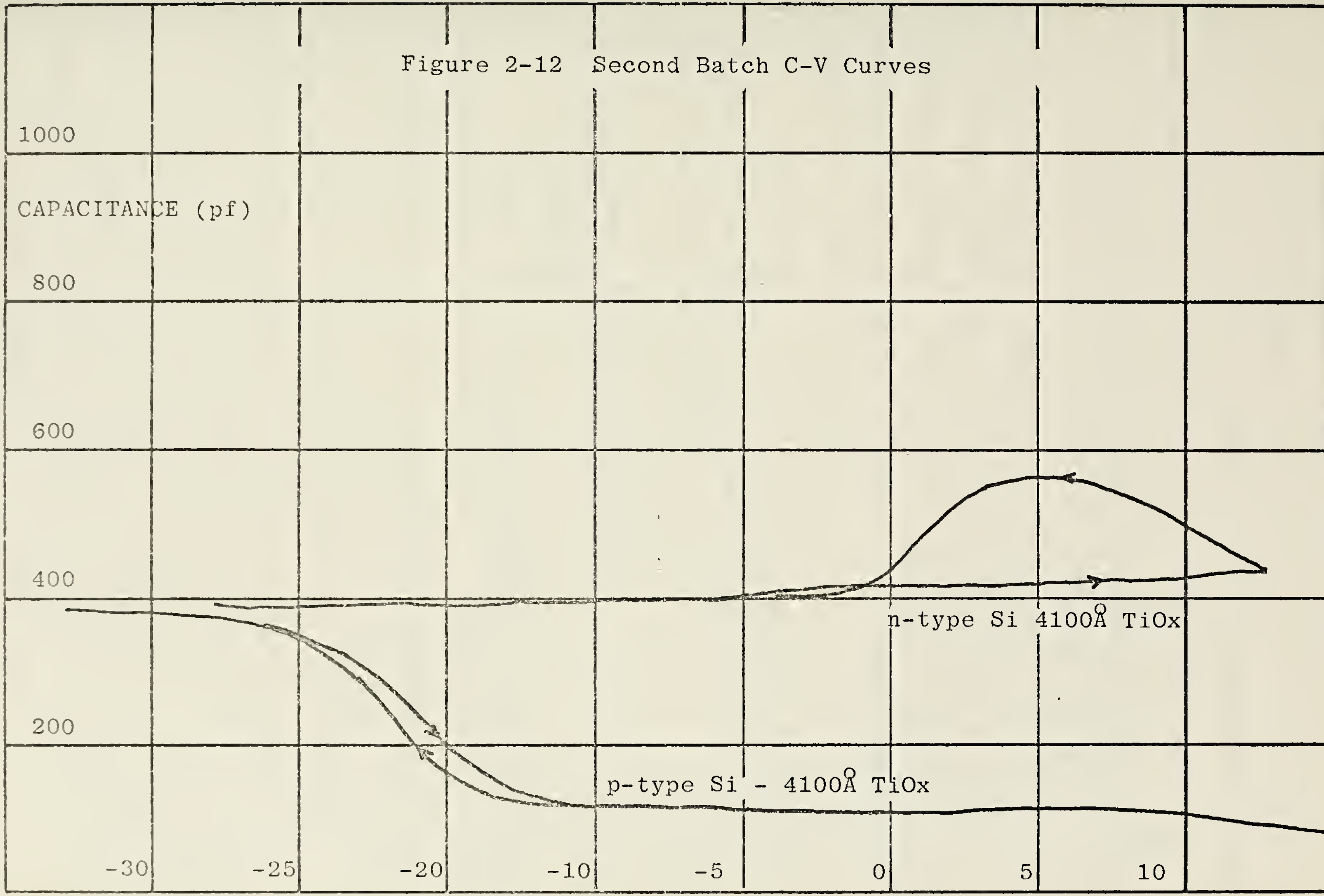


Figure 2-12 Second Batch C-V Curves

but to a larger extent. These samples were made in a different sputtering system from the one used for the first batch of samples. The difference in power supply and target arrangement could have caused the differences in results.

4. Results of the Second Batch Following Heat Treatment

Various heat treatment of these samples were tried. The series of heat treatments included short periods of 300°C in nitrogen atmosphere, three and five minutes in oxygen atmosphere at 800°C, and finally a 16 hour treatment at 280°C in a nitrogen atmosphere. These did not significantly improve the C-V characteristics.

Calculation of the dielectric constant showed that it ranged from 15-20 in the four samples which is again lower than expected for TiO_x.

E. EXPERIMENTAL RESULTS II-IV-VI MIS

1. Thin Films

N-type thin films were obtained with carrier concentrations ranging from 1×10^{17}-2×10^{18}. The mobilities ranged from 2000-25,000 at 77°K. Although two heavily tellurium rich compounds ($PbTe_{1.005}$, $PbTe_{1.001}$) were used as the evaporant source, p-type thin films have not been obtained. To obtain p-type semiconductor films a different furance will have to be constructed which contains two separate chambers with separate heat controls. One chamber will contain PbTe and the other pure tellerium. By controlling the tellurium's temperature the carrier concentration might be better controlled. A typical setup is reported by Kasai.

2. Insulator

Anodization was attempted on several glass slides covered with various thicknesses of titanium metal. A saturated solution of oxalic acid was used as the anodization agent. A thin film of TiO_x film was formed but was very lossy and broke down under applied voltages, typically five volts or less.

To anodize titanium, a constant current (in the vicinity of one microampere/cm) is applied. As time progresses, the voltage increases proportional to the depth of the insulator layer. Typical reported growth rates are 20-25Å of insulator per volt.

Good anodization films can be grown using the apparatus described with the following improvements. A buffer of HCl should be added to the bath to combine with the sodium atoms in the distilled water. The pH value should be monitored and kept lower than 1.0.

III. SYSTEM ANALYSIS

A. INTRODUCTION

When studying infrared imaging it is imperative to study the different noise sources present to discover the limiting factor for operation of the device. In this section three different imaging systems will be compared under many different situations to attempt to show which has more promise. It will also be shown that the new solid state approach to infrared imaging using the CCD and CID are feasible using certain signal processing schemes suggested herein.

The three different systems to be compared are;

i. Linear and Area Array Vidicon

ii. Linear and Area Array CID

iii. Linear and Area Array CCD

Figures of merit used are Noise Equivalent Flux Density (NEFD) which is determined by setting signal current equal to noise current and solving for signal flux, Q_s. Another figure of merit used is Noise Equivalent Temperature Differential (NEΔT), which is NEFD/total differential spectral flux density. An acronym used frequently is BLIP which stands for Background Limited Infrared Photodetection.

Three cases will be presented to demonstrate the capabilities and limitations of infrared imaging. A plot of NEFD and NEΔT versus Q_b will be shown and pertinent data from these plots will be summarized in tables. After these

three cases have been presented, various methods will be proposed to solve the noise limitations of the various systems.

Four spectral regions are used (2.4-2.7μm, 2.7-3.0μm, 3.0-5.5μm, and 8.0-12.5μm), but it should be pointed out that any particular user can readily use the equations presented for his spectral regions to determine specifications for his own system.

Finally, data will be presented in such a way that if a specific mission is desired with a specific spectral region and a certain array size available, one can start a trade off comparison of NEΔT, nonuniformity, readout time and charge storage capacity to determine an optimum system to meet his needs.

B. DEVELOPMENT OF THE EQUATIONS

1. The Two Dimensional Vidicon System

The basic formulas for the noise currents were derived by J. O. Dimmock and are summarized here.

The NEFD due to background

$$(\mathrm{NEFD})_b = \frac{4}{\pi D}\left[\frac{Q_g \Omega_{\mathrm{FOV}}}{2MT_o t_F \eta}\right]^{\frac{1}{2}} \tag{15}$$

The NEFD due to amplifier noise

$$(\mathrm{NEFD})_a = \frac{[2\pi k(T_a+T_L)C_i]^{\frac{1}{2}}}{q\eta G \frac{\pi}{4} D^2 T_o t_F} \tag{16}$$

The NEFD due to array element nonuniformities

$$(NEFD)_n = \frac{gQ_b\Omega_{FOV}}{M\pi} \tag{17}$$

definition of terms

Q_b = background photon flux density

Ω_{FOV} = field of view

D = primary collection optics diameter

M = total number of resolution elements

m = number of rows of elements

n = number of columns of elements

T_o = transmission efficiency of the optics

t_F = frame time

η = retina quantum efficiency

k = Boltzman's constant

(T_a+T_L) = equivalent input temperature of the amplifier plus load resistor

C_i = retina to ground capacitance

q = electronic charge

G = retina photoconductive gain

g = point-to-point rms variation in sensor sensitivity

Two other factors will limit the operation of the vidicon. These are:

a. Beam Starvation

The electron beam current available for infrared vidicon camera tubes can be limited. A beam current of 10μa is assumed for this report.

b. Retina Discharge

Essentially this is saturation of the charge storage capability of the vidicon retina.

2. <u>Linear Vidicon</u>

The basic formulas are similar to those for the two dimensional case but reduced by array sizes.

$(NEFD)_b$ = that for the two dimensional case divided by $n^{\frac{1}{2}}$

$(NEFD)_a$ = that for the two dimensional case with a different value for C_i

$(NEFD)_n$ = that of the two dimensional case

3. <u>Charge Injection Device (CID)</u>

The equations were developed by General Electric.

$$(NEFD)_b = \frac{4}{\pi D^2 T_o} \left[\frac{Q_b T_o A_d}{2F^2 t_i \eta}\right]^{\frac{1}{2}} \tag{18}$$

$$(NEFD)_a = \frac{4}{\pi D^2 T_o} \frac{[2\pi k(T_a+T_L)C_t]^{\frac{1}{2}}}{q t_i \eta} \tag{19}$$

$$(NEFD)_n = \frac{g Q_b \Omega_{FOV}}{M\pi} \tag{20}$$

definition of terms

A_d = size of individual detector elements

t_i = integration time per element

C_t = total input capacitance of the read out amplifier

4. Charge Coupled Devices (CCD)

a. Background Shot Noise

Transfer efficiency (μ) of an n-element array is $\mu = (1-\varepsilon)^{n_g}$ where ε = functional charge loss per transfer and n_g = the number of transfers. For a two-phase CCD n_g equals 2n.

$$(NEFD)_b = \frac{4}{\pi D^2 T_o} \left[\frac{Q_b T_o A_d}{\eta 2F^2 t_i}\right]^{\frac{1}{2}} \tag{21}$$

This equation is the same as in the case of the CID except that η is reduced by μ.

b. Reset and Output Noise

$$(NEFD)_{ro} = \frac{1.4(kTC)^{\frac{1}{2}}}{A_o T_o t_i q \eta} \tag{22}$$

c. Fast Interstate Trapping Noise

$$(NEFD)_{ifs} = \frac{\left[\frac{1.4kTN_{ss} n_g A_g}{q}\right]^{\frac{1}{2}}}{A_o T_o t_i \eta} \tag{23}$$

d. Nonuniformity Noise

$$(NEFD)_n = \frac{g Q_b \Omega_{FOV}}{M\pi} \tag{24}$$

e. Amplifier Limited Noise

This will be identical to equation (19) with η reduced by μ.

definition of terms

N_{ss} = the number of surface states

A_g = the area of the gate

A_o = the area of the optics

C. DESCRIPTION OF THE VARIOUS CASES

1. Case I

This is the ideal case. The integration time of each element is assumed to be 33.3 msec to be compatible with television. This will show what kind of performance can be expected and what is needed to accomplish this.

2. Case II

A charge storage capacity Q_{st} of $1\times10^{13}/cm^2$ is assumed with a readout time of 1×10^{-7} sec (f_{clock} = 10 MHZ) and the largest size array subject to these constraints is used to present results similar to Case I.

3. Case III

A linear array is formed and either mechanically or electronically scanned over the field of view with the frame time equal to 33.3 msec.

4. Useful Graphs

Three useful graphs used in all three cases are presented in figures 3-1, 3-2, and 3-3. Figure 3-1 is a plot of integration time versus Q_b with Q_{st} as a variable. The horizontal line labeled ideal situation is equal to an integration time of 33.3 msec which is compatible to television. Four values of Q_{st} are given. The first two (1×10^{12} and

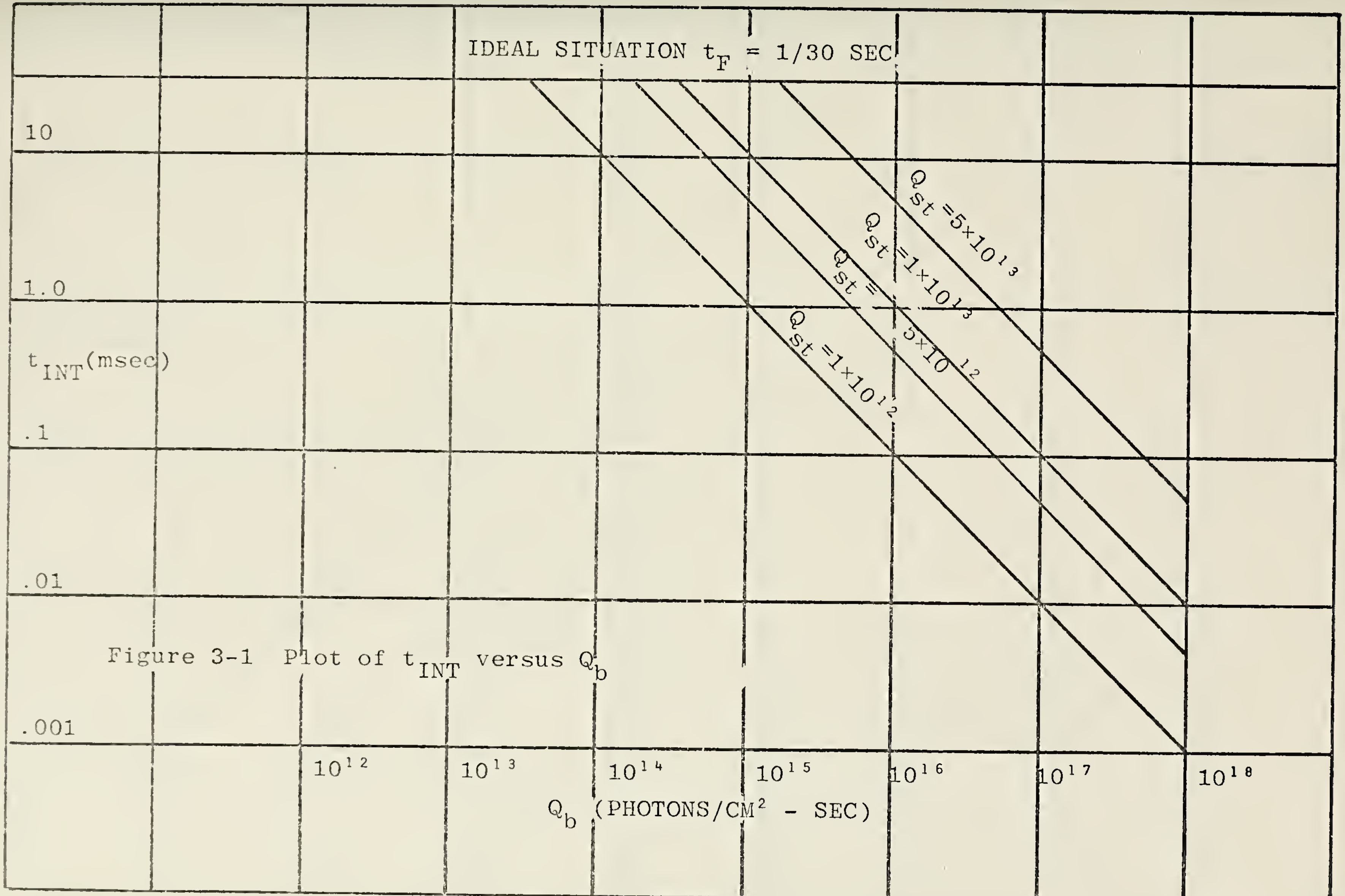


Figure 3-1 Plot of t_{INT} versus Q_b

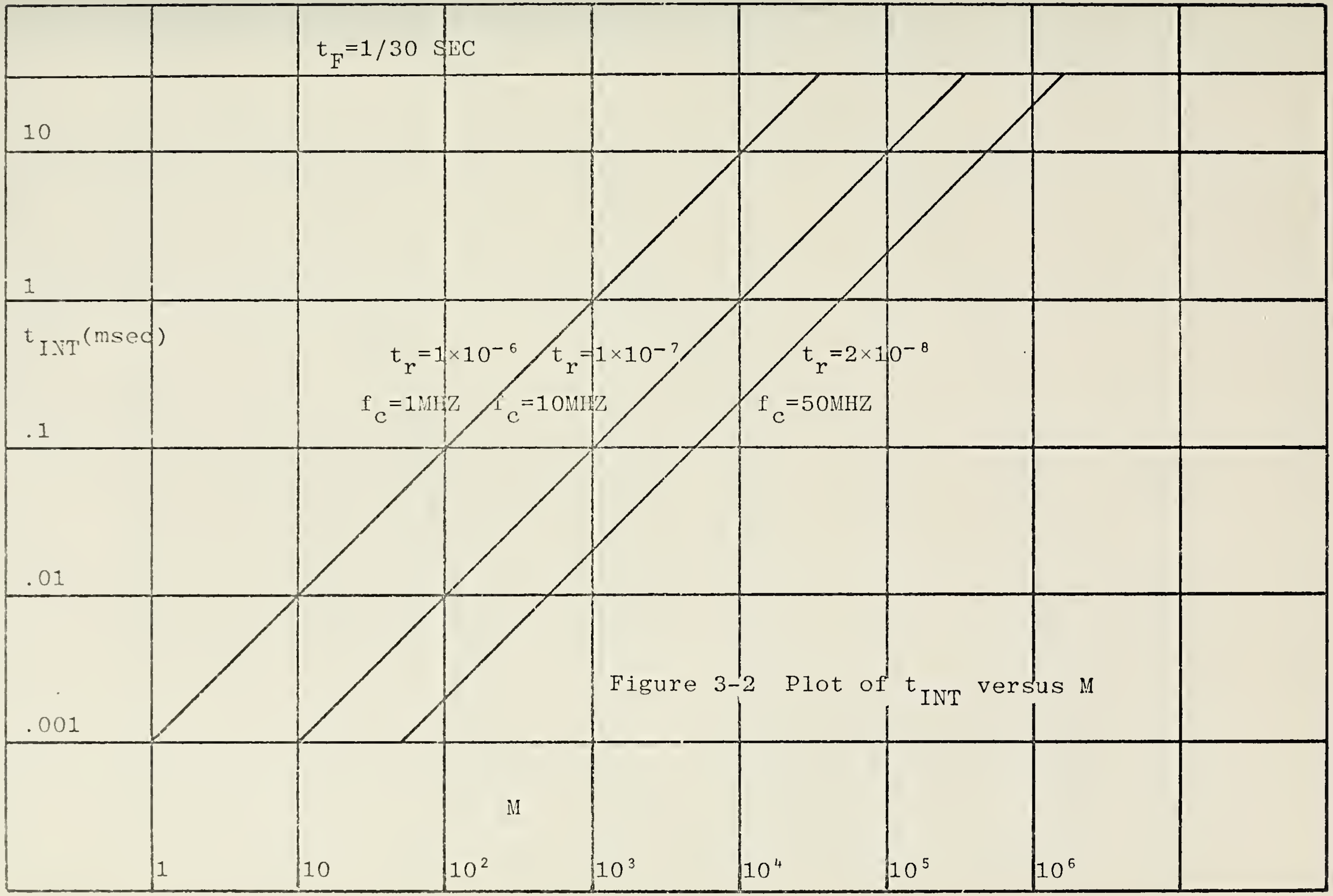


Figure 3-2 Plot of t_{INT} versus M

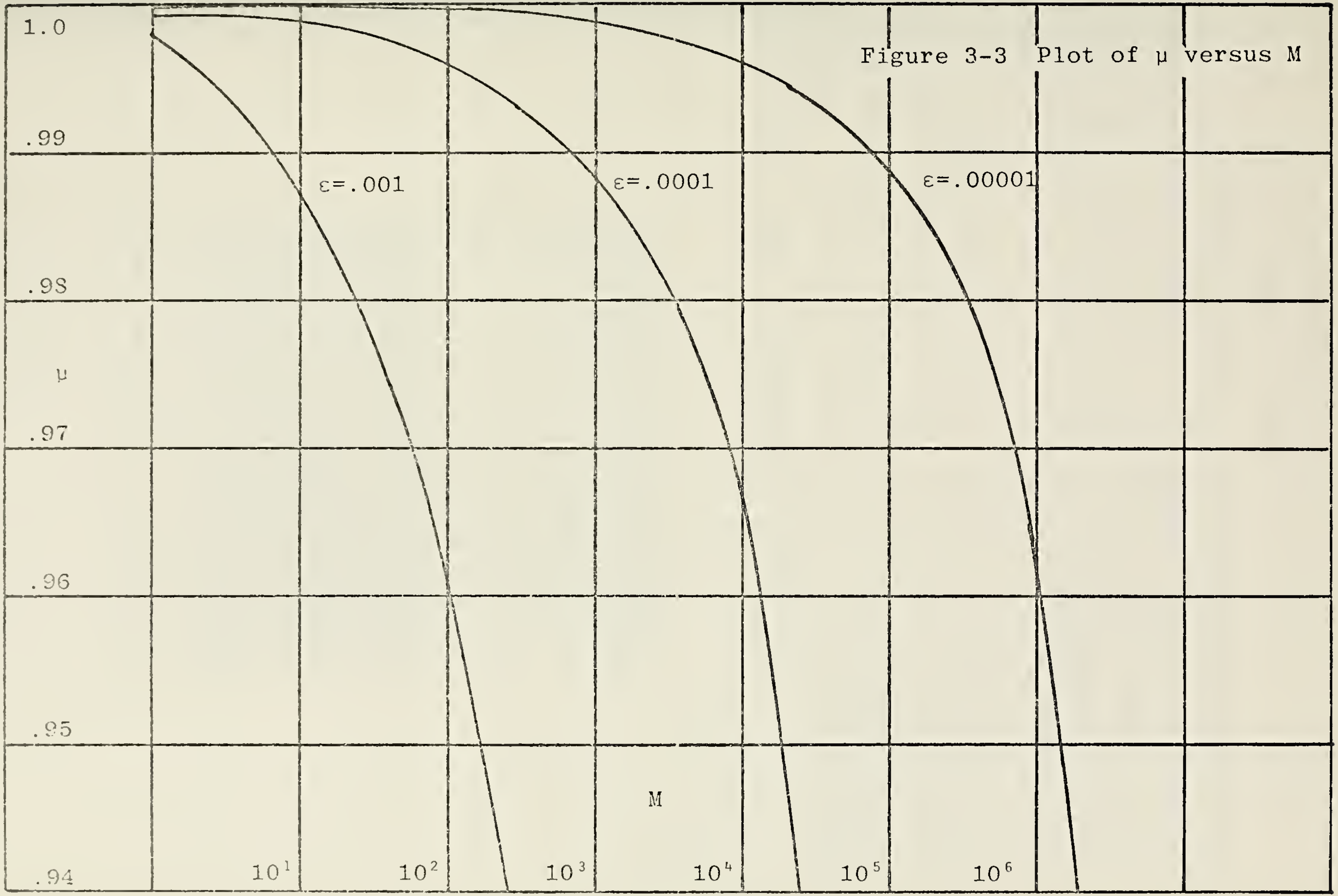


Figure 3-3 Plot of μ versus M

5×10^{12} cm^{-3}) are achievable now and the other two storages in the 10^{13} cm^{-3} range are speculations for the future.

Figure 3-2 is a plot of integration time versus total number of array elements with readout time as the variable. Three clocking times are shown. One and ten megahertz can be achieved presently with 50MHZ being available in the future.

Figure 3-3 is a plot used for the CCD, having transfer efficiency plotted versus total number of array elements with the variable ε which is the fractional charge loss per transfer. The curves plotted are for a two phase CCD using the readout scheme illustrated in figure 3-4.

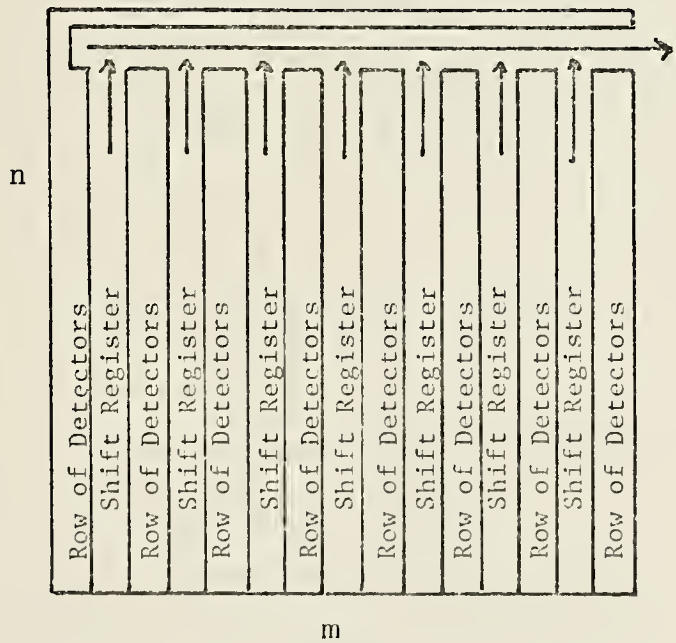


Figure 3-4 Readout Scheme for CCD

The signals in the linear arrays are shifted in parallel into a shift register next to it so that the integration of incoming photons can start again immediately rather than having to wait for the linear array to be read out serially. The parallel shift registers clock the charges into a shift register running horizontally whose clock rate is n times the clock rate of the parallel shift registers.

D. ANALYSIS OF THREE CASES

1. Ideal Case (Case I)

a. System Parameters

t_{INT} = 33.3 msec which is subject to new technology to avoid saturation

$t_r = 1.33\times10^{-7}$ sec $f_{clock} = 7.5$ MHZ

M = 250,000 elements m=n=500

D = 25 cm F = 1.5 $\Omega_{FOV} = (.1\times.1)$ sr

$A_r = \Omega_{FOV} D^2 F^2 = 14.06\ cm^2$

$\eta = G = T_o = .5$

$T_a + T_L = 77°K$

vidicon capacitance = 30 pf

CID capacitance = 10 pf

CCD reset capacitance = .01 pf

CCD capacitance = 10 pf

T_a = atmospheric transmittance = .5

N_{SS} = CCD surface states = 1×10^{11}

b. System Analysis

The system performances were plotted in figure 3-5, a plot of NEFD versus Q_b. The four spectral regions of interest are identified by the background photon flux within their spectral bands. It should be pointed out that in this figure, the background temperature considered is 295°K. The dashed lines are the equivalent NEFD for a NEΔT of .1°K for these four spectral cases. This was chosen as the system performance requirement in this study. It can be seen from figure 3-5 that the 2.4-2.7μm and 2.7-3.0μm systems are limited by amplifier noise from reaching NEΔT = .1°K and the other two systems are nonuniformity limited.

(1) Nonuniformity Limit. Assuming that the amplifier noise can be lowered, Table I lists the maximum nonuniformity tolerable to achieve NEΔT = .1°K.

TABLE I Nonuniformity to Meet NEΔT=.1°K, Case I

$\Delta\lambda$	g
2.4-2.7	.32%
2.7-3.0	.28%
3.0-5.5	.17%
8.0-12.5	.08%

Table II lists the maximum nonuniformity tolerable to achieve the BLIP performance.

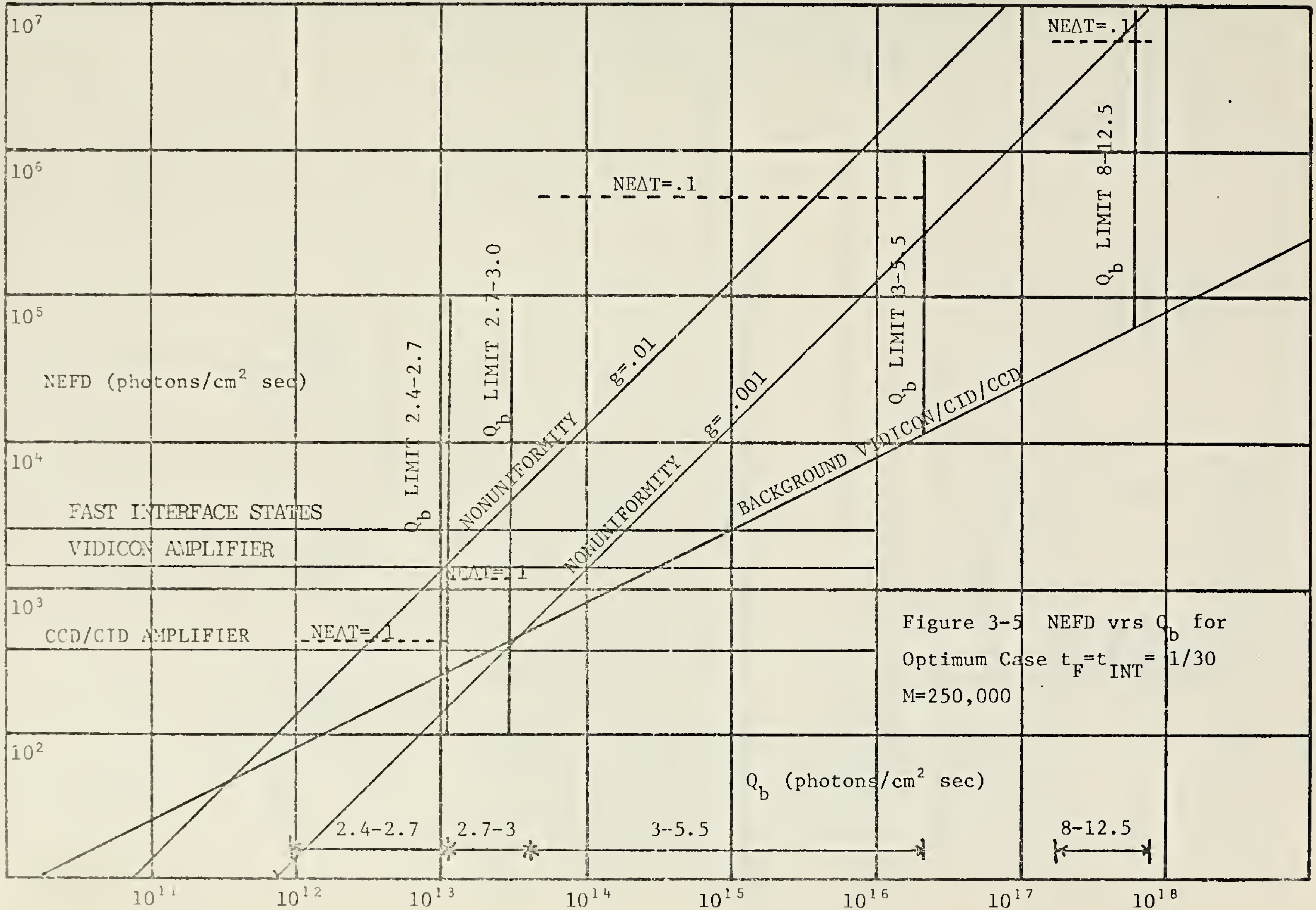


Figure 3-5 NEFD vrs Q_b for Optimum Case $t_F = t_{INT} = 1/30$ M=250,000

TABLE II Nonuniformity to Achieve BLIP, Case I

$\Delta\lambda$	g	Equivalent NEΔT at BLIP (°C)
2.4-2.7	.19%	.0586
2.7-3.0	.11%	.0386
3.0-5.5	.04%	.024
8.0-12.5	.0075%	.0097

The nonuniformity requirements here are severe but it is not likely that a practical system would require NEΔT in the range of a hundredth of a degree or even less. Therefore operation at a NEΔT = .1°K should be adequate.

(2) <u>Amplifier Limited</u>. Table III lists the NEΔT achievable for each system if they are amplifier noise limited. For the CCD, it was bound that the fast interface states noise is larger than the amplifier noise. Therefore, the CCD column in Table III is the fast interface states noise limited. If the amplifier noise limited NEΔT is below .1°K, the NEΔT will be listed just as .1°K.

TABLE III NEΔT if Amplifier Limited, Case I

$\Delta\lambda$	NEΔT Vidicon	NEΔT CID	NEΔT CCD
2.4-2.7	.32	.1	.609
2.7-3.0	.1	.1	.223
3.0-5.5	.1	.1	.1
8.0-12.5	.1	.1	.1

(3) CCD Requirements. For a signal loss of .05 through the CCD, ε must be less than .0000256.

(4) Q_{st} Required to Avoid Saturation. Table IV shows the storage capacity needed to avoid saturation by the background photon flux for an integration time of 33.3 msec.

TABLE IV Storage Capacity Requirements for Case I

$\Delta\lambda$	Allowed t_{INT} for for $Q_{st} = 5\times10^{13}$	Improvement factor to Achieve t_{INT}=1/30	Required Q_{st}
2.4-2.7	4.76 sec	OK	easily met
2.7-3.0	1.55 sec	OK	easily met
3.0-5.5	2.19 msec	15.2	7.6×10^{14}
8.0-12.5	.0775 msec	430	2.15×10^{16}

Other schemes to increase the storage capacity are presented later in this thesis along with schemes to minimize the detrimental effects of nonuniformity.

(5) Conclusions. It is concluded that for infrared solid state imagers for the terrestrial environment detection application with integration time of 1/30 sec and an array size of 250,000 elements that; the 3.0-5.5μm and 8.0-12.5μm imagers will be nonuniformity limited. The 2.4-2.7μm and 2.7-3.0μm imagers will be amplifier limited for IR vidicon and interface state noise limited for CCD. CID amplifier noise limits the 2.4-2.7μm region.

In order to achieve a NEFD equivalent to NEΔT of .1°K for the nonuniformity limited system, the nonuniformity must be less than .17% and .08% for the 3.0-5.5μm

and 8.0-12.5μm imagers. Assuming that the practically achievable nonuniformity is 15%, then some kind of signal processing scheme must be devised to provide the improvement factor of 88 and 212.

In order to achieve a NEFD equivalent to NEΔT of .1°K for the amplifier limited systems, a vidicon amplifier capacitance of 10 pf should be adequate to give a system performance NEΔT of .1°K. However, for the CCD, interface state density less than 10^{11} is needed to achieve NEΔT = .1°K.

It should be noted that it is difficult to accomplish this ideal case with the present technology because integration time may have to be less than 1/30 sec to avoid saturation of the storage element and the array size may have to be smaller than 500×500 because the clock rate is not fast enough to read out the shole array.

2. Charge Storage Limit Case (Case II)

a. System Parameters

The limiting parameter for this case is the charge storage capacity (Q_{st}). It was set equal to $1\times10^{13}/cm^3$ and t_r was set equal to 1×10^{-7} sec (f_{clock}=10MHZ). The longest integration time was chosen to allow the largest array size.

$$D = 25 \text{ cm} \quad F = 1.5 \quad \Omega_{FOV} = (.1\times.1)sr$$

$$A_r = \Omega_{FOV} D^2 F^2$$

$$A_d = A_r/M$$

$$\eta = G = T_o = .5$$

$T_a + T_L = 77°K$

Vidicon capacitance = 30 pf

CID capacitance = 10 pf

CCD reset capacitance = .01 pf

CCD capacitance = 10 pf

$T_a = .5$

$N_{SS} = 1\times10^{11}$

TABLE V Integration Time and Array Size, Case II

$\Delta\lambda$	t_{INT}	M
2.4-2.7	33.3 msec	250,000
2.7-3.0	33.3 msec	250,000
3.0-5.5	.438 msec	4,356
8.0-12.5	.0155 msec	144

Note that for the vidicon t_{INT}=33.3 msec and array size equals 250,000 as the charge storage doesn't depend on Q_{st}.

b. System Analysis

The system performances are plotted in figure 3-6. The dashed lines represent NEΔT = .1°K for each spectral region. Because the plot is rather crowded, the 2.4-2.7μm and 2.7-3.0μm regions are not shown as they are exactly the same as Case I. Therefore all numbers quoted for these regions will be from figure 3-5.

(1) Nonuniformity Limit. If the amplifier noise is disregarded the nonuniformity required to meet NEΔT = .1°K is given in Table VI.

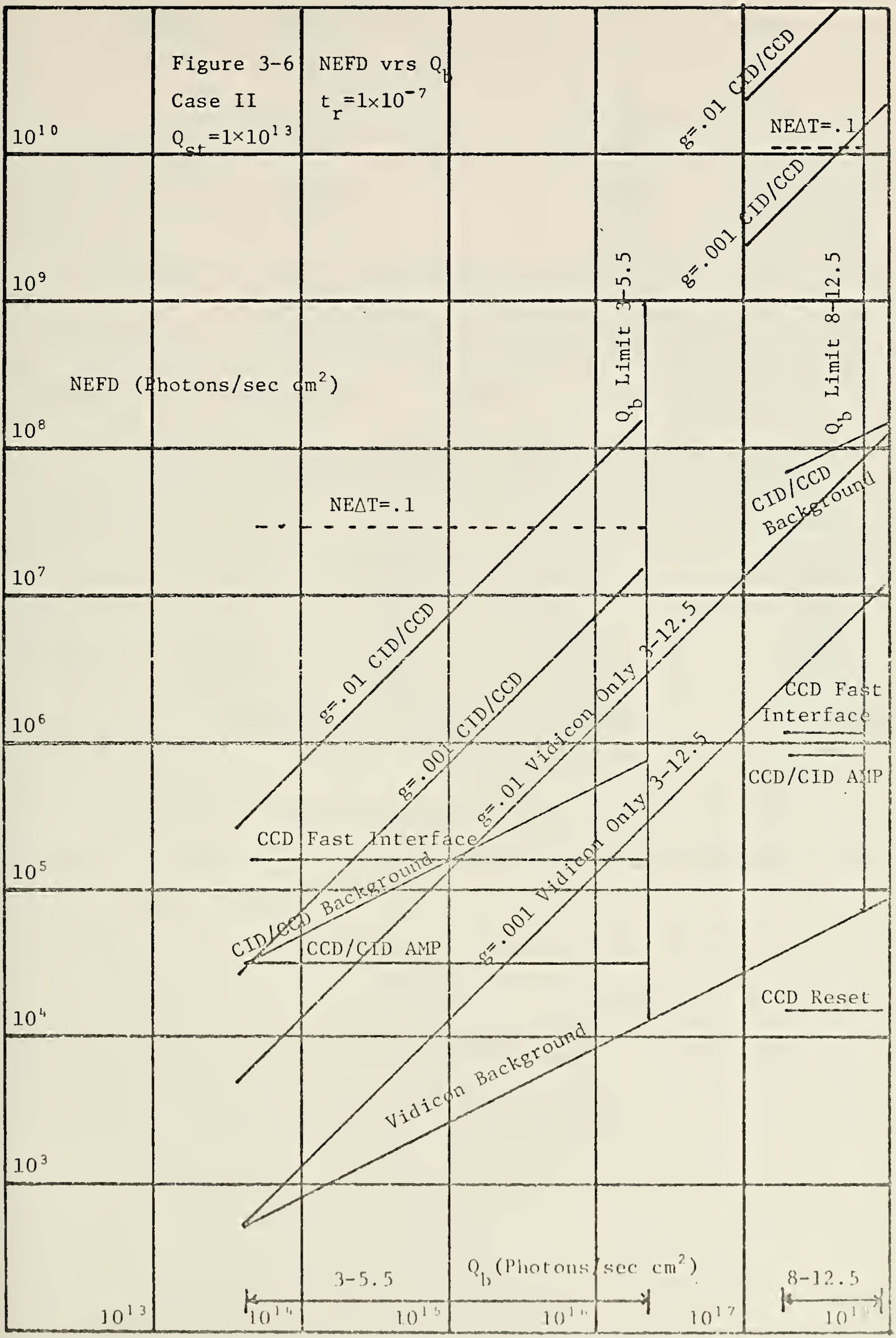


Figure 3-6
Case II
$Q_{st}=1\times10^{13}$
NEFD vrs Q_b
$t_r=1\times10^{-7}$
NEFD (Photons/sec cm^2)
10^{10}
10^9
10^8
10^7
10^6
10^5
10^4
10^3
g=.01 CID/CCD
g=.001 CID/CCD
NEΔT=.1
Q_b Limit 3-5.5
Q_b Limit 8-12.5
CID/CCD Background
g=.01 Vidicon Only 3-12.5
g=.001 Vidicon Only 3-12.5
CCD Fast Interface
CCD/CID AMP
CCD Reset
Vidicon Background
3-5.5
Q_b (Photons/sec cm^2)
8-12.5
10^{13}
10^{14}
10^{15}
10^{16}
10^{17}

TABLE VI Nonuniformity to Meet NEΔT=.1°K, Case II

$\Delta\lambda$	g
2.4-2.7	.32%
2.7-3.0	.28%
3.0-5.5	.17%
8.0-12.5	.077%

In Table VII, the nonuniformity required to achieve BLIP performance is given.

TABLE VII Nonuniformity to Achieve BLIP, Case II

$\Delta\lambda$	g vidicon	g CID/CCD	Equivalent NEΔT at BLIP (°C) vidicon	CID/CCD
2.4-2.7	.19%	.19%	.0586	.0586
2.7-3.0	.11%	.11%	.0386	.0386
3.0-5.5	.000066%	.0046%	.000038	.000038
8.0-12.5	.0000004%	.00085%	.0000005	.0000005

The same considerations have to be taken here as in Case I as to whether it is really needed to have such a small NEΔT.

(2) Amplifier Limit. Table VIII lists the NEΔT achievable for each system if they are operated at the amplifier noise limit. If amplifier noise limited NEΔT is less than .1°K, it will simply be listed as .1.

TABLE VIII NEΔT if Amplifier Limited, Case II

$\Delta\lambda$	NEΔT vidicon	NEΔT CID	NEΔT CCD*
2.4-2.7	.32	.1	.609
2.7-3.0	.11	.1	.223
3.0-5.5	.1	.1	.1
8.0-12.5	.1	.1	.1

* Fast Interface State

(3) CCD Requirements. Table IX list the CCD transfer efficiency required such that the signal will only suffer 5% loss after transferring through the CCD.

TABLE IX CCD Transfer Efficiency

$\Delta\lambda$	μ	ε	μ	ε
2.4-2.7	.95	.000025	-	-
2.7-3.0	.95	.000025	-	-
3.0-5.5	.95	.00019	.975	.0001
8.0-12.5	.95	.001	.995	.0001

(4) Conclusions. In the 2.4-2.7μm and 2.7-3.0μm regions, the CID will be able to meet requirements if non-uniformity can be circumvented. The vidicon will do the same with a little better amplifier performance. The CCD will again need work in surface states. The 3.0-5.5μm and 8.0-12.5μm regions are a different story. Even though all systems are nonuniformity limited at NEΔT = .1°K, it has to be considered how limited in resolution the CCD and CID will be with a 66×66 and 12×12 array.

3. <u>Linear Array (Case III)</u>

a. System Parameters

A 500 element linear array mechanically scanned across the scene.

$t_F = 33.3$ msec

$n = 500$

scan time/line = .0667 msec = t_{INT}

$t_r = 1.33\times10^{-7}$ sec

$D = 25$ cm $F = 1.5$ $\Omega_{FOV} = (.1\times.1)$sr

$A_r = D^2F^2\Omega_{FOV}$

$A_d = A_r/250{,}000$

$\eta = G = T_o = .5$

$T_a+T_L = 77°K$

vidicon capacitance = 30 pf

CID capacitance = 10 pf

CID reset capacitance = .01 pf

CCD capacitance = 10 pf

$T_a = .5$

$N_{SS} = 1\times10^{11}$

b. System Analysis

The system performances are plotted in figure 3-7. The dashed lines represent NEΔT = .1°K for each spectral region. For these cases, the three lower spectral regions are generally amplifier limited because the integration time is so short.

(1) <u>Nonuniformity Limit</u>. Disregarding amplifier noise Table X lists the nonuniformity requirements to achieve a NEΔT = .1°K.

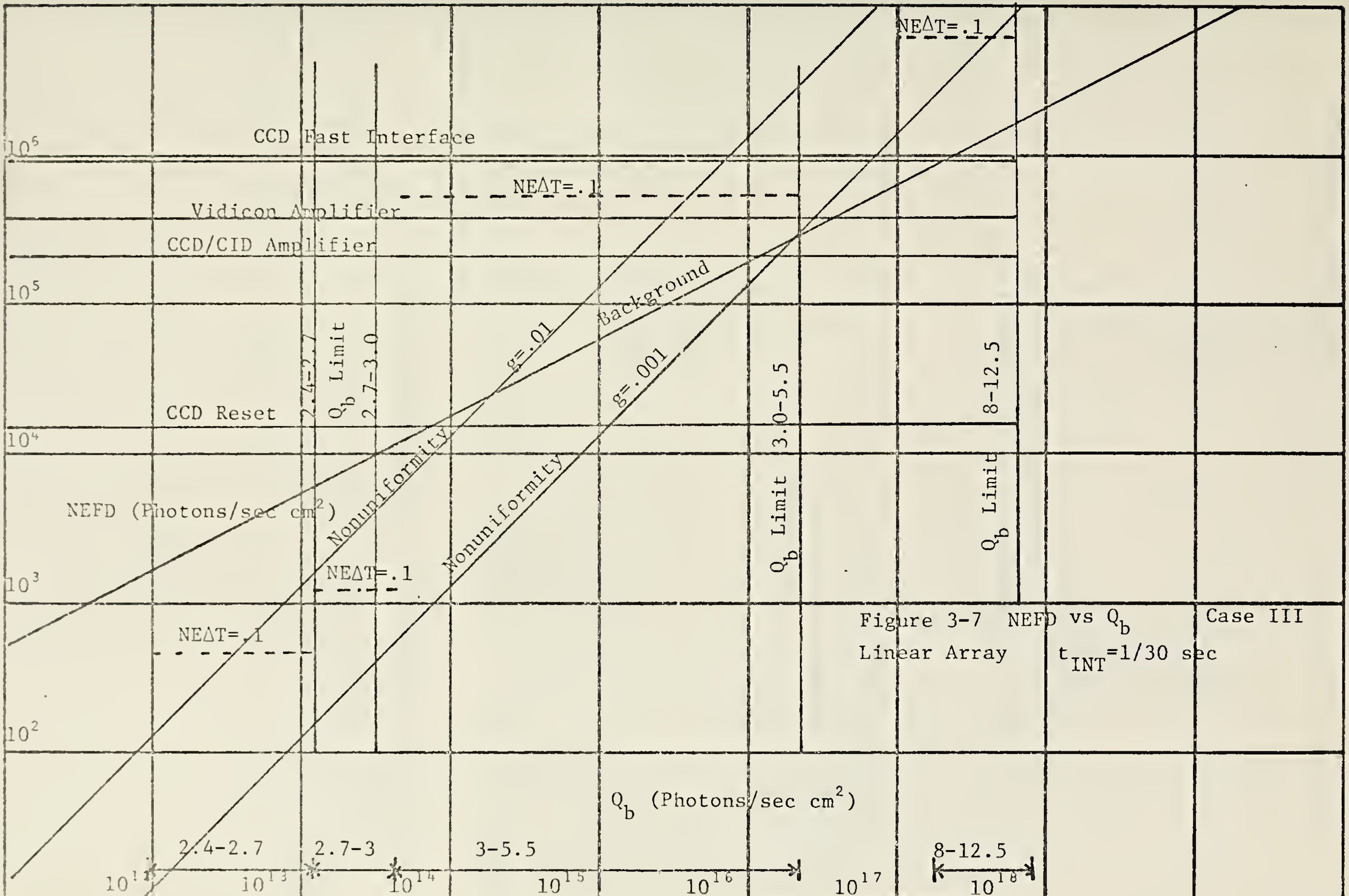


Figure 3-7 NEFD vs Q_b Case III
Linear Array $t_{INT}=1/30$ sec

TABLE X Nonuniformity to Meet NEΔT=.1°K, Case III

$\Delta\lambda$	g
2.4-2.7	.32%
2.7-3.0	.28%
3.0-5.5	.17%
8.0-12.5	.078%

Table XI lists the nonuniformity requirements to achieve the BLIP performance.

TABLE XI Nonuniformity to Achieve BLIP, Case III

$\Delta\lambda$	g	Equivalent NEΔT at BLIP (°C)
2.4-2.7	4.1%	1.29
2.7-3.0	2.4%	.86
3.0-5.5	.089%	.5
8.0-12.5	.017%	.02

Note in three of these cases, NEΔT = .1°K is below the BLIP performance. Therefore, it will be impossible to achieve NEΔT = .1°K.

(2) Amplifier Limited. Table XII lists the equivalent NEΔT if amplifier noise limits the performance. Again, the NEΔT will be listed as .1 if the amplifier limited NEΔT comes out less than .1°K.

TABLE XII NEΔT if Amplifier Limited, Case III

$\Delta\lambda$	NEΔT vidicon	NEΔT CID	NEΔT CCD*
2.4-2.7	113	46	218
2.7-3.0	42	16	80
3.0-5.5	.1	.1	.187
8.0-12.5	.1	.1	.1

* Fast Interface State

Note that the two shorter spectral regions have ridiculously large amplifier limited NEΔT's.

(3) <u>CCD Requirements</u>. For a transfer loss of .05, ε must be .000052 or less.

(4) <u>Conclusions</u>. This linear array is clearly not as good as the area array because of the short integration time. A possible solution is to construct an area array using m linear arrays, each made up of shorter linear arrays. By using these in a staggered mode of operation, longer integration time can be achieved with better performance.

E. SCHEMES TO IMPROVE DETECTOR ARRAY PERFORMANCE

Much of these ideas to improve detector array performance are originated in a General Electric Report on Background Suppression.

1. <u>Improvement of Storage Capacity</u>

a. Increasing the Storage Area

To increase the charge storage capacity, the target detector area is held constant but the volume of the

storage cell is increased by increasing the storage area. A mask is placed over the extra area that is not acting as a detector to prevent photons from penetrating. Defining K as the ratio of enlarged storage area to active area, it can be shown that the maximum background flux, Q_b, allowable is increased by this factor of K.

b. DC Bias Removal

In this region of the spectrum the background photon flux is several orders of magnitude larger than the signal photon flux. Therefore if this background can be partially removed, the integration time can be increased. A method of accomplishing this is shown in figure 3-8. After the well is partially filled, a portion of the signal is skimmed off and transferred into a storage well that is protected from photon flux by a special mask. This skimming off process is repeated as amny times as necessary to achieve the specified frame time. This process is applicable to both the CID and CCD but not the vidicon. This method should be easily applied to linear arrays. For area arrays, there may be some difficulty due to the increased size of the three gate array.

The specifics of operation are as follows. By external adjustment the amount of voltage applied to the transfer gate and thus the amount of charge transferred is controlled. As shown in figure 3-8, at time t_3, the amount of charge left in the receiver cell should be equal to the background charge at the temperature of operation. This

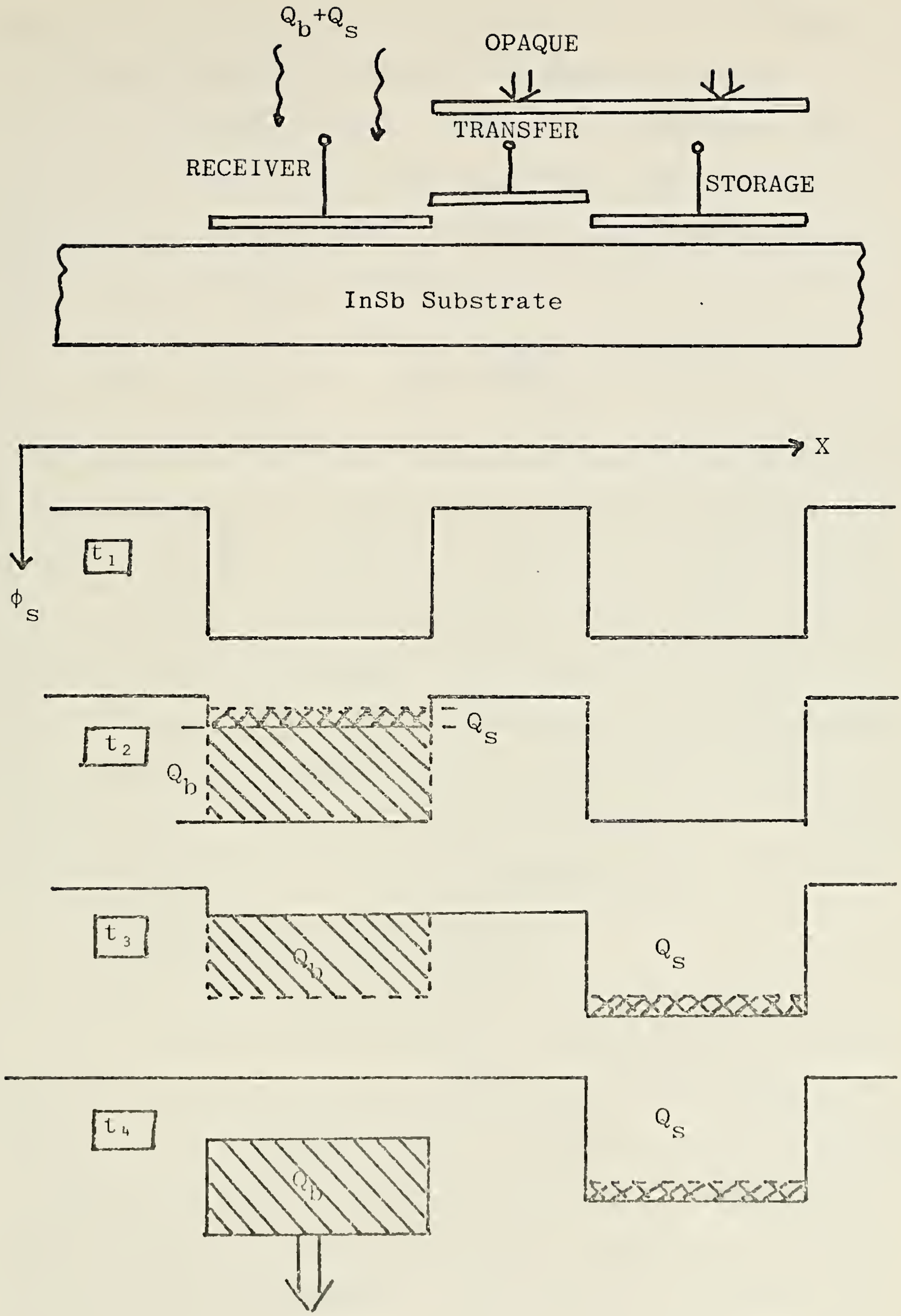


Figure 3-8 Operation of Multi-Gate Structure

controls the size of the storage cell which also depends on the charge storage capacity of the semiconductor.

Letting ΔQ equal the amount of charge transferred each time, j equal the number of times charge is transferred, and F_z equal the ratio of fat zero at the receiver cell to total cell capacity,

$$\Delta Q j = F_z Q_{st} \qquad \Delta Q = \frac{F_z Q_{st}}{j}$$

F_z is set by the operator by illuminating the detector array with a blackbody or looking at a scene that is mostly background. Since Q_{st} is known, a trade off can then be made between ΔQ and j. ΔQ determines the large signal end of the dynamic range of the imager. The small signal end of the dynamic range is the NEΔT = .1°K which is the minimum temperature difference discernable. The ΔQ discussed here is related to the greatest temperature difference in the scene the imager can detect before blooming occurs.

2. Nonuniformity Compensation

a. Individual Amplifiers

The simplest method to compensate for a nonuniformity is to read out each element into its own amplifier. The array is illuminated with a blackbody and each amplifier is adjusted to give a uniform presentation. From time to time the amplifiers would have to be readjusted to correct for drifts and degradations. This method is theoretically the best but in most cases costly to implement, especially in an area array due to fabrication difficulties and space limitations.

b. Adjustment of Parallel Analog Channels

The signal from a linear array is read out serially and amplified by an integrating preamp and then demultiplexed into parallel channels which are then low pass filtered. The pads following the low pass filters are adjusted to give a constant presentation from a blackbody. Again the pads have to be readjusted from time to time to correct for variations in time. Figure 3-9 shows a block diagram of this scheme. This is simpler to implement than method 1 above since an amplifier isn't required for each element but one for each linear array. The design of its length is closely related to the integration time. This method is applicable to both CID and CCD's.

c. Read Only Memory (ROM) Method of Correction

This scheme employs a ROM to record the nonuniformity of each cell and they in turn control the gain of a variable gain amplifier as each element is read out. Figure 3-10(a) shows how the nonuniformity is stored in the ROM when the array is under constant illumination. Figure 3-10(b) shows the scheme in operation.

The following discussion will determine how much improvement one can expect from such an arrangement. Since this is a digital scheme, the exact correction for g cannot be made. Assuming that the reference signal is equal to one of the signals of the array and $g = 0.1$, the range of the gain of the amplifier must be $2\times[1/(1-g)] = 2.22$.

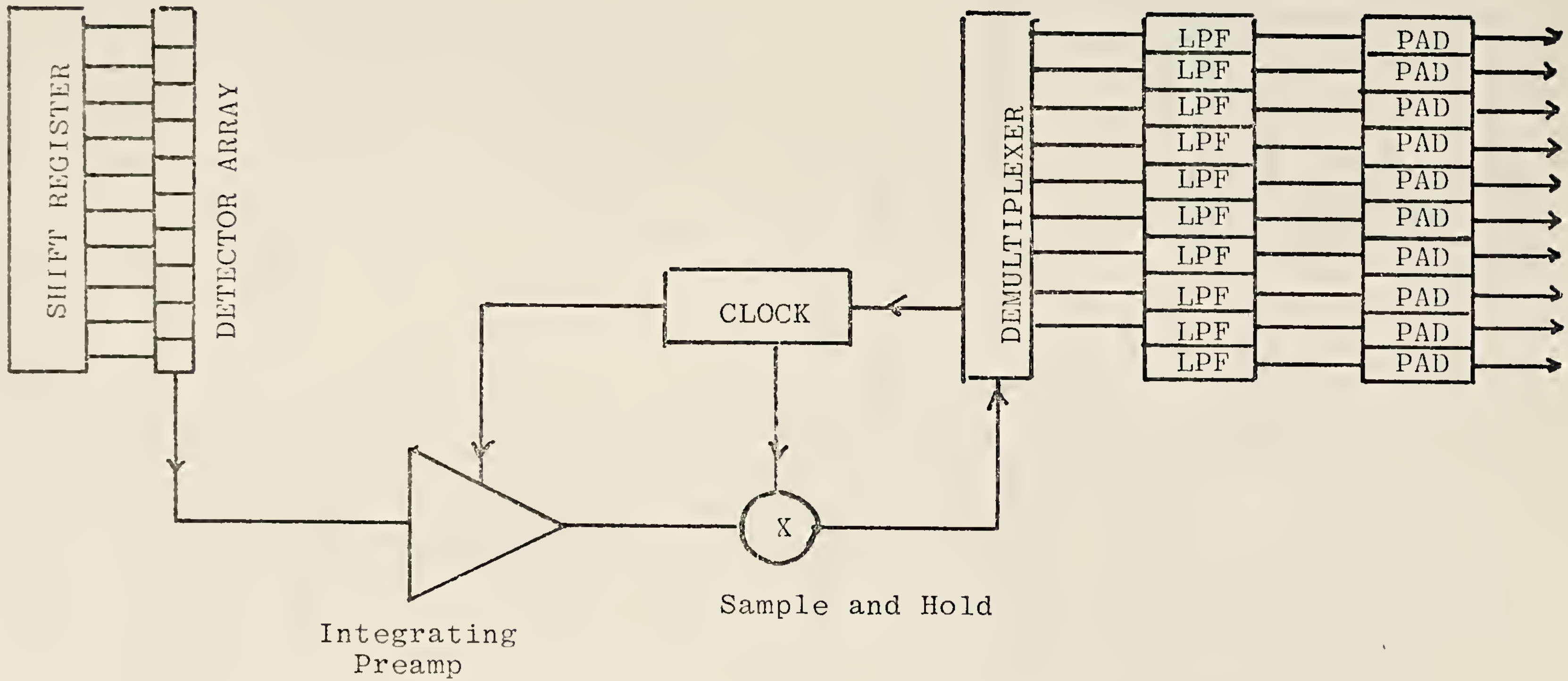
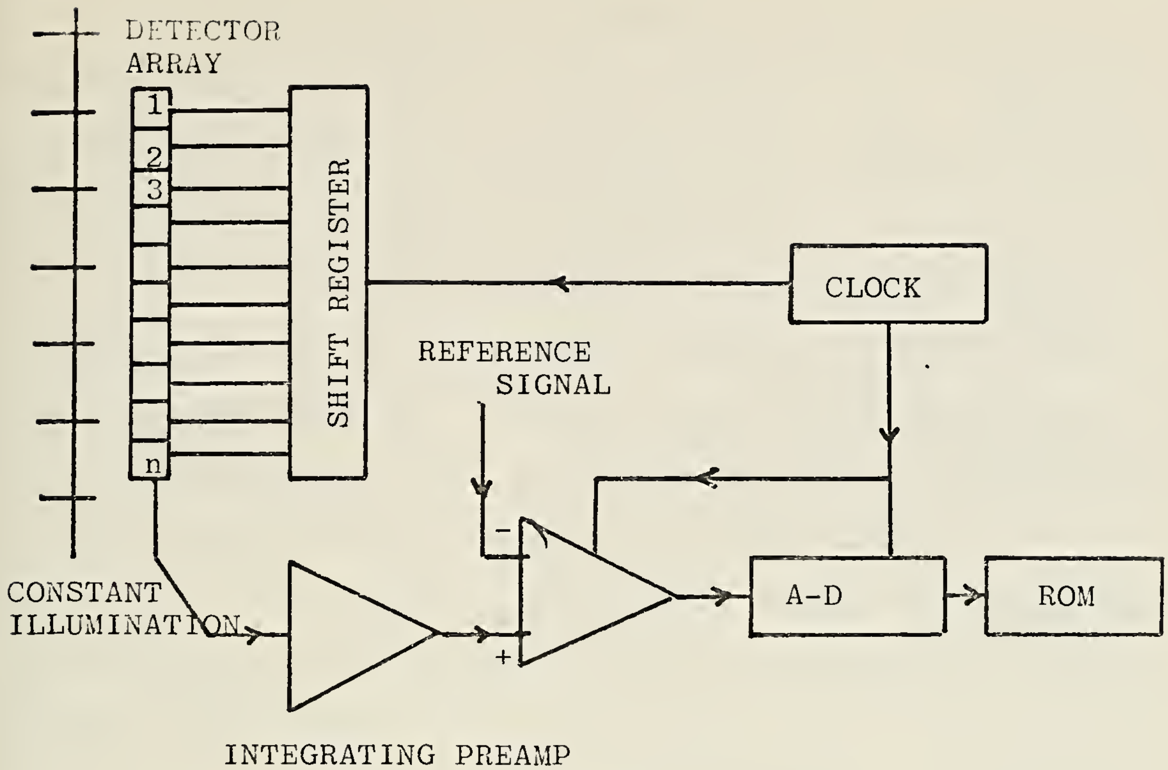
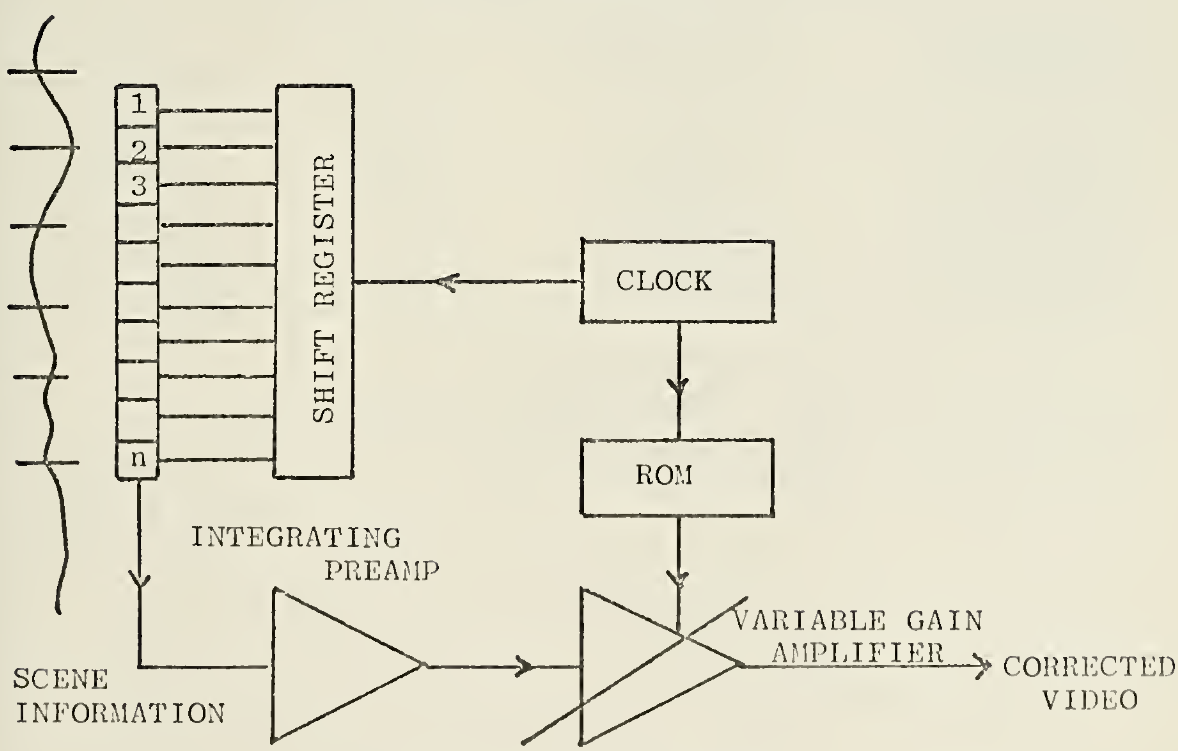


Figure 3-9 Block Diagram of One-Dimensional CID/CCD System with Parallel Processing



(a) Responsivity Measurement



(b) Signal Measurement

Figure 3-10
Block Diagram of ROM Method to Correct Nonuniformity

The accuracy or smallest number that g can be limited to is dependent on the number of bits of ROM used to store each element's nonuniformity. For example, four bits are necessary to improve g to 10% or .1.

Each case studied previously will be investigated to see what size of ROM is needed to improve their performance to NEΔT = .1°K or to reach BLIP conditions. It is assumed that g = 0.5 is the worst case of nonuniformity to be expected from a practical detector array.

(1) Case I Improvement. Table XIII summarizes the number of bits of ROM needed per element and array to reach NEΔT = .1°K.

TABLE XIII ROM Requirements, Case I

$\Delta\lambda$	g	ROM/element	ROM/array
2.4-2.7	.32%	9 bits	2.25 megabits
2.7-3.0	.28%	9 bits	2.25 megabits
3.0-5.5	.171%	10 bits	2.50 megabits
8.0-12.5	.078%	11 bits	2.75 megabits

(2) Case II Improvement. Table XIV summarizes the number of bits of ROM needed per element and array to reach a NEΔT = .1°K.

TABLE XIV ROM Requirements, Case II

$\Delta\lambda$	g	ROM/element	ROM/array
2.4-2.7	.32%	9 bits	2.25 megabits
2.7-3.0	.28%	9 bits	2.25 megabits
3.0-5.5	.17%	10 bits	43,560 bits
8.0-12.5	.078%	11 bits	1,584 bits

(3) Case III Improvement. Table XV summarizes the bits of ROM needed to operate the linear array at BLIP which is a more meaningful system performance than NEΔT=.1°K in this case.

TABLE XV ROM Requirements, Case III

$\Delta\lambda$	g	ROM/element	ROM/array
2.4-2.7	4.1%	5 bits	2,500 bits
2.7-3.0	2.4%	6 bits	3,000 bits
3.0-5.5	.089%	11 bits	5,500 bits
8.0-12.5	.017%	13 bits	6,500 bits

d. Time Delay Integration (TDI)

A more complicated scheme to improve nonuniformity is to have multiple linear arrays perpendicular to the scan direction. If the signals from these multiple arrays are added with proper phasing to add the signals from the same target coherently, the nonuniformity effect can be averaged and system sensitivity can be enhanced by the square root of the number of TDI elements used. This method is particularly effective if the arrays have a constant gradient

of nonuniformity along the linear array as two with similar gradients can be arranged, so their scan linearities run opposite one another and will cancel. Figure 3-11 shows a block diagram of this scheme.

e. Automatic Gain Control

A limiting feature in the above scheme is the A-D and D-A conversions and the large ROM size required. It is desirable to develop a system where the gain of the correcting amplifier is controlled by analog signals. Therefore the solution is to store the nonuniformity signal from a blackbody illumination in a capacitor which would control a variable gain amplifier. If the capacitor would retain its full charge this would minimize the effects of nonuniformity effectively. However, the limiting factor here is the RC time constant of the capacitor, since $(1-g) = e^{-t/RC}$. The charges on the capacitors used for correcting the nonuniformity will have to be reset periodically.

F. DEVELOPMENT OF AN ANALYSIS TOOL FOR DESIGNING AN INFRARED SYSTEM

In this analysis, the equations developed in section III-B are used and certain basic parameters are set. These are:

$\eta = T_o = .5$

$D = 25$ cm $\quad F = 1.5 \quad \Omega_{FOV} = (.1\times.1)$sr

$T_a + T_L = 77°K$

CID capacitance = 10 pf

CCD reset capacitance = .01 pf

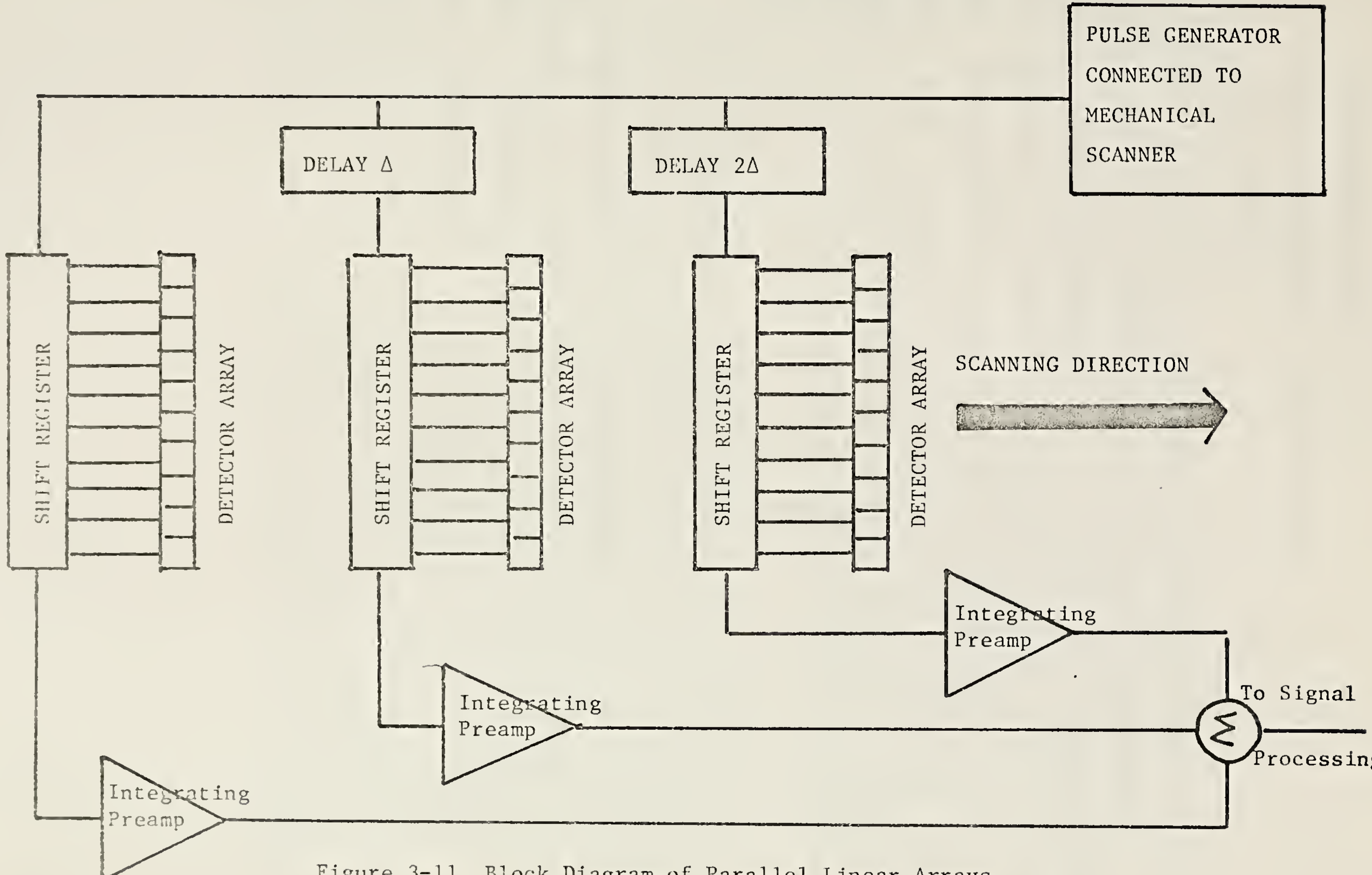


Figure 3-11 Block Diagram of Parallel Linear Arrays

CCD capacitance = 10 pf

T_a = atmospheric transmittance = 0.5

$N_{SS} = 1\times10^{11}$

The analysis consists of two parts as described below. The system used is for imaging in the 3.0-5.5μm region which given a limiting background of $Q_b = 2.28\times10^{16}$ photons/sec-cm^2 and a signal $Q_s = 3.9\times10^{14}$ photons/sec-cm^2 for a 2π field of view. Using the relationships between NEFD, NEΔT, and Q_s, figure 3-12 is plotted for various values of NEΔT with total number of elements and NEFD as the two variables. Superimposed on this plot are lines for various values of nonuniformity, g.

When designing an infrared system either NEΔT or M will be known. Using one of these parameters figure 3-12 is used to determine the other parameter making sure that the nonuniformity can be met or an improvement package such as the ROM or AGC can meet this and still meet other system parameters such as weight, power consumption, and cost. After this information is obtained, figures 3-1, 3-2, and 3-3 must be consulted to make decisions as to charge storage capacity, integration time, readout time, and CCD transfer efficiency.

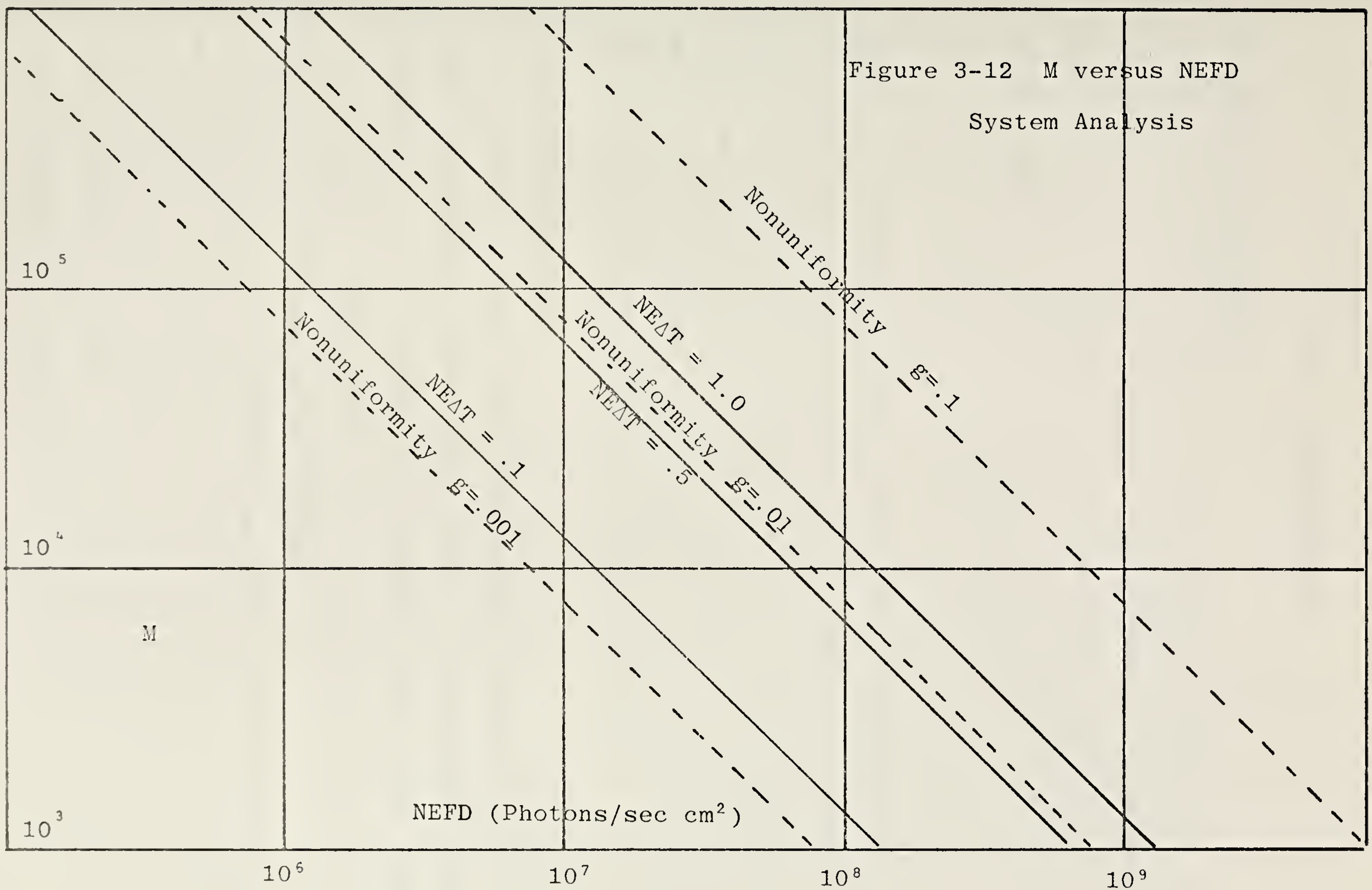


Figure 3-12 M versus NEFD
System Analysis

IV. CONCLUSIONS

A. DEVICE FABRICATION

To successfully image in the infrared, a basic unit of the imager, the charge transport device must be developed. This includes a semiconductor with an energy gap compatible to the spectral region of interest and a high dielectric insulator for large charge storage capability.

A thin film PbTe semiconductor was developed successfully. A titanium dioxide insulator was developed with encouraging insulator properties. With continuing effort in developing the anodization method, device quality insulator films can be developed. After fabricating the insulator and semiconductor together and applying a metal contact, this MIS capacitor should exhibit good MIS properties.

B. SYSTEM ANALYSIS

A study of various infrared imaging systems was undertaken to determine their noise limitations and their system performances. The systems included the vidicon, CCD, and CID. Spectral regions investigated included the 2.4-2.7μm, 2.7-3.0μm, 3.0-5.5μm, and 8.0-12.5μm.

The first case studied assumed that each detector element was capable of an integration time of 33.3 msec to be compatible with real time television type of display. For system performance of NEΔT = .1°K, the four spectral regions were nonuniformity limited for CID operation. For the

vidicon and CCD, the two short wavelength regions were amplifier noise and fast interface states limited, respectively. For the two longer wavelength regions, they were nonuniformity limited.

The second case assumed a charge storage capacity and readout time which are practical within the present day technology. The largest array size was chosen subject to these constraints. For the two lower wavelength regions, integration time can be 33.3 msec and the array size is 250,000 elements. Thus their limitations were the same as in the first case. It was much different in the two longer spectral regions as integration time was severely limited by the large background photon flux, thus limiting the array sizes to 4356 and 144 elements, respectively. Therefore, the NEΔT performance analysis carried out in this thesis must be extended and combined with an analysis of imaging quality such as the MTF and the spatial resolution calculations, which have not been done in this thesis.

The third case studied involved a linear array scanned across the scene mechanically. Because of the short integration times, the amplifier noise limited performance in all but the longer spectral regions. The method to avoid this difficulty is to construct an area array of many linear arrays. By staggering them, the integration time can be increased and thus system performance can be improved.

Various methods of improving system performance were discussed [Ref. 11]. Increasing the storage area and using

dc blocking were two methods to increase the charge storage capability and thus integration time. The three gate device for dc blocking provides the greatest promise.

Several methods were suggested to minimize the detrimental effects of nonuniformities. These included individual amplifiers for each element, adjustment of parallel analog channels, read only memories (ROM), time delay integration, and automatic gain control (AGC). Of these methods, the AGC has the most promise as it can achieve more accurate nonuniformity improvement using fewer components.

Finally, a method was suggested to meet the requirements for a particular system. By plotting a few basic equations, tradeoffs can be made between various system parameters to develop the optimum infrared imaging system for that particular application.

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